



May 21, 2013 07:45 AM Central Daylight Time

Si2's OpenDFM Standard Gains Industry Support

Technical contributions help drive standards for multi-company demos at DAC

Design Automation Conference 2013

AUSTIN, Texas--(BUSINESS WIRE)--The Silicon Integration Initiative (Si2) announced today that several leading semiconductor and EDA companies have voiced their commitment to adopt Si2's OpenDFM standard version 2.0. The OpenDFM standard describes an open, high-level language that can generate popular verification runsets for use in any major EDA design for manufacturability (DFM) verification tool. OpenDFM allows designers to maintain one EDA-tool independent source for DFM checks.

"OpenDFM v2.0 is a significant step forward in the efficiency of maintaining multiple runsets for different DRC engines," says Tim Rost, Ph.D., Director, CMOS Design Enablement, Texas Instruments, Inc. "This is particularly advantageous given that we utilize several DRC vendors across our design space. A second advantage of this methodology is that it provides a framework for writing easily codeable rule checks. We've tested plug-ins from all of the major EDA vendors and found very good performance, accuracy, quality and consistency of results. Currently we are utilizing OpenDFM generated runsets in both production and development design environments."

"The Unified Layer Model (ULM) functions are an essential component in the Polygon Operator OpenAccess API extensions"

"IBM has been using OpenDFM as the specification language of choice for reflecting our data prep retargeting operations in our production extraction flows in the 22nm and 14nm technologies," says James Culp, Manager - Design Rules and Implementation, Design Technology Integration, IBM. "The ability to specify one algorithm in an open standard language which converts to multiple vendor implementations has reduced our design kit development costs, without any impact on performance or quality. Additionally, IBM is specifying Design Rule Manual (DRM) content in OpenDFM format to enable DRM consistency checking and for improved PDK automation."

"Mentor is pleased to continue working with Si2 to expand and further define OpenDFM, which is based upon Mentor's and TSMC's original donation of the iDRC architecture to the industry," said Michael White, Director of Product Marketing, Calibre Physical Verification Products. "For this latest v2.0 release, Mentor contributed to the definition, verification, and alignment of the rules with practical use models to facilitate adoption across the industry."

The latest release, OpenDFM v.2.0, includes:

- New Targeting functions that optimize manufacturing yield on problematic patterns
- Design Rule Manual (DRM) consistency checking and PDK automation
- Production-level support for 28nm process nodes and development support for 20nm nodes
- Support for the Unified Layer Model that is used by OpenDFM, OpenPDK and OpenAccess Extensions.

"The Unified Layer Model (ULM) functions are an essential component in the Polygon Operator OpenAccess API extensions," says James Masters, PDK Infrastructure Manager, Technology and Manufacturing Group, Intel Corp."The ULM functions

provide a rich set of layer operations which can be used as building blocks for developing robust flows on leading-edge process technologies. By leveraging an industry standard, we can ensure that ULM functionality will be well-tested and consistent across multiple design flows and EDA software."

"The latest version of OpenDFM can play a major role in improving the efficiency and quality of physical verification and DFM," says KT Moore, Group Director, Silicon Signoff and Verification, Silicon Realization Group at Cadence. "Closing the productivity gap for physical verification at 20nm and below requires more manufacturing awareness than ever before. OpenDFM has become a successful, common, open format that can be translated to the native languages of several DRC engines with no loss of fidelity."

The OpenDFM 2.0 standard, which is available to the public at no charge, can be obtained at this link: https://www.si2.org/www_site_map.php#DFMC . Members of the DFMC also have access to substantial adoption collateral, such as the OpenDFM parser source code, contributed test cases, tutorials, demonstration code, and more. To access this adoption collateral and to participate in the next phase of OpenDFM enhancements, please join the DFMC. See this link for more information: <http://www.si2.org/?page=491>.

Many Si2 member companies have made significant technical contributions to help create current and future versions of the OpenDFM standard. Examples include: IBM (test cases), Intel (Pattern Generator), GlobalFoundries (DRC+), Mentor Graphics (iDRC), STMicroelectronics (Example45 DRC), Synopsys (ITF), Texas Instruments (test cases) and TSMC (iDRC).

Please come by Si2's booth #1427 at the Design Automation Conference in Austin, TX, June 2-6, where several presentations will present more details on OpenDFM. A complete schedule is located at: <http://www.si2.org/?page=1651>.

About the Design For Manufacturability Coalition (DFMC)

DFMC's charter is to specify open standards for software interfaces between EDA software tools and manufacturing software. The specification includes standard terminology definitions, semantics and exchange formats for relevant manufacturing information. It also includes standard software application program interfaces (API) for models describing different manufacturing processes, yield mechanisms and circuit behaviors. Member companies include: Cadence Design Systems (NASDAQ: CDNS), GLOBALFOUNDRIES, IBM (NYSE: IBM), Intel Corporation (NASDAQ: INTC), LSI (NYSE: LSI), Mentor Graphics (NASDAQ: MENT), Polyteda, Samsung Electronics (KSE:005930), STMicroelectronics (NYSE:STM), Synopsys (NASDAQ: SNPS), Tela Innovations, Inc., and Texas Instruments (NYSE: TXN).

About Si2

Si2 is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. Now in its 25th year, Si2 is uniquely positioned to enable timely collaboration through dedicated staff and a strong implementation focus driven by its member companies. Si2 represents over 80 companies involved in all parts of the silicon supply chain throughout the world. See www.si2.org.

All product, company and institution names are trademarks or registered trademarks of their respective owners.

Contacts

Silicon Integration Initiative
William Bayer, 512-342-2244, ext. 304
Senior Director, Marketing Communications



