The Future of Low Power

Low Power is the Future

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Predicting 15 years into the Future is Difficult

“I think there is a world market for maybe five computers”
Thomas Watson, IBM

“There is no reason anyone would want a computer in their home”
Ken Olsen, DEC

“640K ought to be enough memory for anybody”
Bill Gates, Microsoft
Looking back 15 years from 2015

- We stand in the year 2015 and look back to the year 2000
  - Looking into the past from 2015 gives us a much better view
  - Politicians still selectively recall what they knew or what they said
  - We ended the Power Format Wars and started convergence
  - Energy Efficiency became a key metric for data centers & mobile

- We see the trends that began in Year 2000 fully played out
  - New waves of integration were enabled via Block Level reuse
  - Greater process variability required tighter control of chip operation
  - Customers begin to value Low Power more than Clock Speed
  - Millions of transistors finally realize the “SoC” defined in year 2000
Year 2015: The Low Power Agenda

- Why Low Power became the new “Currency” in the electronics industry
- Why the natural (physical) trends in power, performance and manufacturing variability required greater control
- The Format Wars are Over and a New Age has begun!
- Why CPF became the Gold Standard for Low Power Design Intent
In Year 2000: Clock Speed was a “Currency”

Currency = Clock Speed was widely accepted as a quality with a priced value.
But Leakage Became a Much Bigger Issue

![Graph showing power density vs. gate length for different years. The graph indicates that leakage power dominates as gate lengths decrease, with a significant increase in leakage power between Year 1985 and Year 2015.](image-url)
And the World went **GREEN**

**Lower Power Reduces Cost** of both Operation and Cooling

Bus 2GHz, Clock Speed 2.5GHz
Cache 512KB x2, 65nm
Lower Power is Priced Higher

<table>
<thead>
<tr>
<th>45W</th>
<th>65W</th>
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<tbody>
<tr>
<td>$25</td>
<td>$</td>
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</table>

Operating Cost 1 in California = \$0.12/KWHr

45W Athlon 4805e vs 65W 4800e list price difference for 65nm AMD Dual Core at 1K units

90W Cooler = \$65
Year 2015: Low Power is the “New Currency”

Currency = Low Power is now widely accepted as a quality with a priced value

Clock Speed (at Power)

- Over Power Bin
- Over Cooling or Over Battery Capacity Limit
- Market Price at Speed Bin

- Leff
- Faster
- Slower

- 3.0 GHz
- 2.0 GHz

Leakage Power Dominates Power Profile

- $20.00 Less
- $15.00 Less

45W

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Low-Power Design at AMD

**Chip Details:**
- SoC has 23 power domains, 21 On/Off, 2 Always-On
- Used footer power switches
- In On/Off tiles, there are Always-On RAMS
- Used AND function isolation cells
- Used always on buffer/inverter
- Two power modes

**Approach:**
- CPF used as the *Golden Power Intent* across the entire design flow:
  - RTL & gate simulation, implementation, chip assembly, verification
- Top-down hierarchical CPF generation solution:
  - Full-chip CPF & Block-level CPF’s for LP implementation of blocks
- Formal equivalence as low power verification solution across entire design flow:
  - Complete RTL, logical, and physical checking / top-level, block-level, and final chip assembly
Year 2015: The Low Power Future

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Manufacturing Variability was Out-of-Control

Power Variability \(=\) Profitability

Without better control, power variability becomes too large

Low Power Techniques with CPF reduced power variation

Power Variability

Year 1995

Year 2005

Year 2015

Year of Introduction

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# CPF Reduced Out-of-Control Power Variations

<table>
<thead>
<tr>
<th>Low Power Control Technique</th>
<th>Power Impact</th>
<th>CPF Controls</th>
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</thead>
<tbody>
<tr>
<td>Optimized Buffers, Level Shifters, Isolation</td>
<td>+/- 10%</td>
<td>Define Power Rules, Verify Control</td>
</tr>
<tr>
<td>Clock Tree Optimization and Clock Gating</td>
<td>+/- 20%</td>
<td>IR Drop Limits, Gating Verification</td>
</tr>
<tr>
<td>Multi-Threshold Library Optimization</td>
<td>+/- 30%</td>
<td>Multiple Libraries, Temperature</td>
</tr>
<tr>
<td>Dynamic Voltage Frequency Scaling</td>
<td>+/- 30%</td>
<td>Mode Transitions, Verify Control</td>
</tr>
<tr>
<td>Multi-Voltage Islands with Shut-off, Stand-by</td>
<td>+/- 30%</td>
<td>Power Modes, Illegal Configuration</td>
</tr>
<tr>
<td>Adaptive Body Bias (on leakage current only)</td>
<td>+/- 40%</td>
<td>Define Bias Lines, Verify Control</td>
</tr>
<tr>
<td>ESL Prototype, Verification, Implementation</td>
<td>+/- 60%</td>
<td>Operating Corners, Group Mode/View</td>
</tr>
</tbody>
</table>
Year 2000: New Waves of Integration Began

Body Weight

Exercise

Blood Pressure

Asthma Air Flow

Blood Glucose

Previously Integrated

Alcohol Blood Content
Year 2015: iPhone is the First Medical Tricorder

New

Old

ECG Transmission

Tricorder Model TR-560
New Integration: Hierarchy Support was Key!

Chip Top-Level
- Top Level Integrated CPF’s

Memories
- New IP CPF

Hard IP (RTL/Behavioral)
- New IP CPF

Hard IP (w/RTL or gates)
- Reused IP CPF

Soft IP (RTL)
- Reused IP CPF
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New Integration: Low Power Design Intent

Top-Down Hierarchy

Chip Top-Level

Top Level CPF

Block 1

Block 2

Block 3

Block 4

Silicon Integration Initiative
## CPF 1.1: Extensions over CPF 1.0

### Integration: Hierarchy Enhancements

<table>
<thead>
<tr>
<th>Feature</th>
<th>CPF 1.0</th>
<th>CPF 1.1</th>
</tr>
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<tbody>
<tr>
<td><strong>Bottom Up Hierarchy</strong> control for third party IP integration and reuse</td>
<td></td>
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<tr>
<td>User defined <strong>Macro Models</strong> for multiple instances of Block level IP</td>
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<tr>
<td><strong>Secondary Supplies</strong> for State Retention, Isolation Cells, Always-on Buffers</td>
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<tr>
<td><strong>Stand-By State</strong> Added to Off State and On State</td>
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<tr>
<td>Grouping of Power Domains with <strong>Group Modes</strong> and <strong>Group Views</strong></td>
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<tr>
<td><strong>Macro Modeling</strong> (Behavioral Level) of Hard IP such as Embedded Memory</td>
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<tr>
<td>Transition Slope, Latency and Cycles for <strong>Power Domain Transitions</strong></td>
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<tr>
<td>User defined assertion of <strong>Illegal Power Modes</strong> and <strong>Illegal Shut Off Conditions</strong></td>
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<tr>
<td>Syntax and Semantic Enhancements recommended by the LPC members</td>
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Legend: New Feature ○  Extended Feature ○  **Italics** New CPF Terminology
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Years 2006 - 2009: The Power Format Wars

- Two giants battled with tremendous powers
- But the low power landscape was severely trampled
- Complex issues are never really **Black** and **White**
  - Both formats had their strong and weak points
  - In the end, cooperation was better for everyone
Interoperability with P1801:

CPF 1.2 File

CPF 1.2 Parser

Translator Functions
- Name mapping
- Power modes and states
- Power supply sets
- Supply functions
- Rules and strategies

P1801 File

P1801 Parser

CPF 1.2 Data Model

Bidirectional Translator

P1801 Data Model
Compatible Subset

1 A subset of P1801 commands cannot be translated. User guidance will be provided until the ambiguities are resolved.
Cooling Down the Power Format Wars

• **Identify a common Command Set used in both P1801 and CPF**
  - Consistently describe Low Power design intent to drive optimization, verification and implementation
  - Bi-directional translation (CPF 1.2 + design) & (P1801 + design)
  - Resolve ambiguities between the compatible subsets

• **Start to converge the data models of P1801 and CPF 1.2**
  - Complete and release a Open Power Data Model specification
  - Provide guidance for commands outside of translatable subset

• **Focus on the Industry Requirements for the best standard**
  - Improve Block Level IP modeling and representation
  - Build a standard that is better than either P1801 or CPF 1.0
  - Incorporate LPC feedback from CPF 1.0 and CPF 1.1

• **Reach out to P1801 Supporters and work together**
  - Many of the original P1801 supporters adopted CPF
Year 2015: The Low Power Agenda

- Why Low Power became a new “Currency” in the electronics industry
- Why the natural (physical) trends in power, performance and variability needed intervention
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Industry-wide Adoption of CPF

Silicon Integration Initiative

- Industry Leaders
  - FJITSU
  - NEC
  - Freescale
  - NXP
  - STARC
  - WIPRO
  - LSI

- Foundry Reference Flows
  - TSMC
  - UMC
  - SMIC

- IP Vendor Support
  - ARC
  - VIRAGE
  - Linari
  - ARM
  - MIPS
  - Tensilica
  - Sonics

- EDA Integration
  - Cadence
  - Calypso
  - Sequence
  - AFRENIA
  - Azuro
  - Magma

- Design Services
  - Faraday
  - Motech
  - Synopsys
  - Synopsys
  - Cadence
  - Synopsys

- ASIC
  - FJITSU
  - NEC
  - LSI
  - ZIS

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It was easy to get started in Advanced Low-Power

**A Practical Guide to Low-Power Design**

- **Contents:**
  - Low-power methodology
  - Captures collective effort of 36 Power Forward Initiative members
  - 9 User experience chapters by ARM, ARC, Faraday, Freescale, Fujitsu, NEC Electronics, NXP, Sequence and TSMC
  - 3 new chapters published 12/2008

Free download from: www.powerforward.org
5000+ Downloads!
CPF Support Grew a Large Ecosystem

2008 Adoption Aids in the Si2 library:

2009 Adoption Aids in the Si2 library:
Fujitsu Proved it Worked!

**Verified with test design**
- PSO functional verification with full simulation
- Low power structural and physical check (Shifters/Isolators/Power switches)
- Domain aware place and route

**Conclusion**
- Functional verification is necessary for complex PSO design for design bugs
- Structural check with CPF could verify LP design
- Fujitsu will support CPF-based ASIC flow for their customers

**Silicon Proven in September 2007**

- 90nm
- 940K instances
- 11 Power Domains
- 19 Power Modes
What’s in Your Future?

- **CPF Evolution**
  - Complete **CPF 1.2** Enhancement List 10/2009
  - Complete and release the **Open Power Data Model** specification 03/2010

- **CPF Support**
  - Complete all support materials for the **CPF 1.1 Enhancements**
  - Begin Support for CPF 1.2 in 3Q - 4Q/2009

- **CPF Related Events:**
  - Low Power Seminar 05/2009
  - Design Automation Conference: 07/2009
  - EDS Fair 01/2010
Conclusions from the Year 2015

- **CPF was established as the Gold Standard low power format**
  - Adopted world-wide by EDA companies and by 100+ design teams
  - Proven record of success based on first time silicon at Speed & Power

- **CPF evolved as a industry standard driven by the real life requirements from key stake-holders in the LPC**
  - CPF 1.0, CPF 1.1 and CPF 1.2 Enhancement Roadmaps were clearly defined and achieved their target release dates

- **Si2 helped Low Power to become the New Currency**
  - Wiki-based collaborative standards for Low Power Design Web-enabled adoption support for Europe, Asia and United States
  - Rich collection of Low Power adoption aids
  - Multiple Si2-sponsored Low Power events
本当にありがとうございます
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