The Future of Low Power

Low Power is the Future

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Si2, Inc.

Innovation Through Collaboration
Predicting 15 years into the Future is Difficult

“I think there is a world market for maybe five computers”
Thomas Watson, IBM

“There is no reason anyone would want a computer in their home”
Ken Olsen, DEC

“640K ought to be enough memory for anybody”
Bill Gates, Microsoft
Looking back 15 years from 2015

- We stand in the year 2015 and look back to the year 2000
  - Looking into the past from 2015 gives us a much better view
  - Politicians still selectively recall what they knew or what they said
  - We ended the **Power Format Wars** and started convergence
  - **Energy Efficiency** became a key metric for data centers & mobile

- We see the trends that began in Year 2000 fully played out
  - New waves of integration were enabled via **Block Level** reuse
  - Greater process variability required **tighter control** of chip operation
  - Customers begin to value **Low Power** more than **Clock Speed**
  - Millions of transistors finally realize the “**SoC**” defined in year 2000
Year 2015: The Low Power Agenda

- Why Low Power became the new “Currency” in the electronics industry
- Why the natural (physical) trends in power, performance, manufacturing variability and integration required greater control
- The Format Wars are Over and a New Age has begun!
- Why CPF became the Gold Standard for Low Power Design Intent
オープニング

• 15年後を予測することは非常に困難。

• 2015年から過去15年を振り返る。
  - パワー・フォーマット議論は終了し、収束へ。
  - データ・センター、モバイルの分野では、エネルギーの効率化が重要な測定基準。

• 2000年代に起きたトレンド。
  - ブロック・レベルの再利用により、新しいインテグレーションが可能。
  - プロセスのバラツキはチップを動作させる上で厳しい制御が必要となってきた。
  - 顧客の価値はクロック・スピードから低消費電力へ。
  - "SoC"の台頭。
なぜ低消費電力が電気産業の中で新しい基準となってきたのか？

パワー、パフォーマンス、製造のバラツキ、そして製品化の変遷に対する高度な制御の必要性

フォーマットの議論の終焉と新たな時代の到来！

低消費電力設計指針の標準としてのCPFの現状
Year 2015: The Low Power Agenda

• Why Low Power became the new “Currency” in the electronics industry

• Why the natural (physical) trends in power, performance, manufacturing variability and integration required greater control

• The Format Wars are Over and a New Age has begun!

• Why CPF became the Gold Standard for Low Power Design Intent
In Year 2000: Clock Speed was a “Currency”

Currency = Clock Speed was widely accepted as a quality with a priced value
But Leakage Became a Much Bigger Issue

Power Density (W/cm²) vs. Gate Length (Microns)

- **Active Power**
- **Leakage Power**

Year 1985
Year 2000
Year 2015

Leakage Power Dominates

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And the World went **GREEN**

**Lower Power Reduces Cost** of both Operation and Cooling

**Bus 2GHz, Clock Speed 2.5GHz**
Cache 512KB x2, 65nm

Lower Power is Priced Higher

<table>
<thead>
<tr>
<th>45W</th>
<th>65W</th>
</tr>
</thead>
<tbody>
<tr>
<td>$25</td>
<td></td>
</tr>
</tbody>
</table>

**Operating Cost** in California = $0.12/KWHr

**45W Athlon 4805e vs 65W 4800e list price difference for 65nm AMD Dual Core at 1K units**

90W Cooler = $65
Year 2015: Low Power is the “New Currency”

Currency = Low Power is now widely accepted as a quality with a priced value

Leakage Power Dominates Power Profile

Clock Speed (at Power)

- Over Power Bin
  - $20.00 Less
  - Over Cooling or Over Battery Capacity Limit
  - 45W

- Over Cooling or Over Battery Capacity Limit
  - 2.0 GHz Under Speed Bin
  - $15.00 Less

- 3.0 GHz
  - Market Price at Speed Bin

Faster  \( L_{\text{eff}} \)  Slower
Low-Power Design at AMD

Chip Details:
- SoC has 23 power domains, 21 On/Off, 2 Always-On
- Used footer power switches
- In On/Off tiles, there are Always-On RAMS
- Used AND function isolation cells
- Used always on buffer/inverter
- Two power modes

Approach:
- CPF used as the Golden Power Intent across the entire design flow:
  - RTL & gate simulation, implementation, chip assembly, verification
- Top-down hierarchical CPF generation solution:
  - Full-chip CPF & Block-level CPF’s for LP implementation of blocks
- Formal equivalence as low power verification solution across entire design flow:
  - Complete RTL, logical, and physical checking / top-level, block-level, and final chip assembly
なぜ低消費電力が電気産業の中で新しい基準となってきたのか？

- 2000年初頭: クロック・スピードが価格設定の重要であった。
  - マイクロ・プロセッサーでは2~3GHzの間がマーケットの適正。
  - 3GHz以上でプラス$30、2GHz以下でマイナス$15の価格差。

- プロセスの進化に伴いLeakage Powerがより支配的に。

- スペック的に同等でパワーが20W違う製品の場合、約$25の価格差。
  (例 AMD 4805e: 45W vs 4800e: 65W)

- 現在〜2015年: 消費電力も価格設定のための重要な要素。
  - 2~3GHzの製品であっても、低消費電力化すれば$20の低価格が実現可能。

- AMD 4805eの設計で、CPFを使った低消費電力設計を採用。
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Silicon Integration Initiative

Manufacturing Variability was Out-of-Control

Power Variability = Profitability

Without better control, power variability becomes too large

Low Power Techniques with CPF reduced power variation

Year of Introduction

Year 1995

Power Variability

Max Power

Max Power

Typical Power

Max Power

Typical Power

Power (Watts)

100%

30%

10%

30%

10%
## CPF Reduced Out-of-Control Power Variations

<table>
<thead>
<tr>
<th>Low Power Control Technique</th>
<th>Power Impact</th>
<th>CPF Controls</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimized Buffers, Level Shifters, Isolation</td>
<td>+/- 10%</td>
<td>Define Power Rules</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Verify Control</td>
</tr>
<tr>
<td>Clock Tree Optimization and Clock Gating</td>
<td>+/- 20%</td>
<td>IR Drop Limits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Gating Verification</td>
</tr>
<tr>
<td>Multi-Threshold Library Optimization</td>
<td>+/- 30%</td>
<td>Multiple Libraries, Temperature</td>
</tr>
<tr>
<td>Dynamic Voltage Frequency Scaling</td>
<td>+/- 30%</td>
<td>Mode Transitions</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Verify Control</td>
</tr>
<tr>
<td>Multi-Voltage Islands with Shut-off, Stand-by</td>
<td>+/- 30%</td>
<td>Power Modes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Illegal Configuration</td>
</tr>
<tr>
<td>Adaptive Body Bias (on leakage current only)</td>
<td>+/- 40%</td>
<td>Define Bias Lines</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Verify Control</td>
</tr>
<tr>
<td>ESL Prototype, Verification, Implementation</td>
<td>+/- 60%</td>
<td>Operating Corners</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Group Mode/View</td>
</tr>
</tbody>
</table>
Year 2000: New Waves of Integration Began

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Body Weight
Blood Pressure
Exercise
Blood Glucose
Asthma Air Flow
Alcohol Blood Content

Previously Integrated
Year 2015: iPhone is the First Medical Tricorder

ECG Transmission

Tricorder Model TR-560

New

Old
New Integration: Hierarchy Support was Key!

- **Chip Top-Level**
  - Top Level Integrated CPF’s

- **Memories**
  - New IP CPF

- **Hard IP (RTL/Behavioral)**
  - New IP CPF

- **Hard IP (w/ RTL or gates)**
  - Reused IP CPF

- **Soft IP (RTL)**
  - Reused IP CPF

**Bottom-Up Hierarchy**

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New Integration: Low Power Design Intent

Top-Down Hierarchy

Chip Top-Level

Top Level CPF

Block 1

Block 2

Block 3

Block 4

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## CPF 1.1: Extensions over CPF 1.0

### Integration: Hierarchy Enhancements

<table>
<thead>
<tr>
<th>Feature</th>
<th>CPF 1.0</th>
<th>CPF 1.1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bottom Up Hierarchy</strong> control for third party IP integration and reuse</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>User defined <strong>Macro Models</strong> for multiple instances of Block level IP</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Secondary Supplies</strong> for State Retention, Isolation Cells, Always-on Buffers</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Stand-By State</strong> Added to Off State and On State</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Grouping of Power Domains with <strong>Group Modes</strong> and <strong>Group Views</strong></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Macro Modeling</strong> (Behavioral Level) of Hard IP such as Embedded Memory</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Transition Slope, Latency and Cycles for <strong>Power Domain Transitions</strong></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>User defined assertion of <strong>Illegal Power Modes</strong> and <strong>Illegal Shut Off Conditions</strong></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Syntax and Semantic Enhancements recommended by the LPC members</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: New Feature [✓] Extended Feature [✗] *Italics* New CPF Terminology

**Innovation Through Collaboration**
パワー、パフォーマンス、製造のバラツキ、そして製品化の変遷に対する高度な制御の必要性

• 製造バラツキは消費電力に大きく影響。
  - パワーを考慮しない設計: 消費電力は2倍(100%)
  - 低消費電力化を考慮した設計: 消費電力は1.3倍(30%)

• CPFを使った低消費電力設計により、パワーのバラツキを削減。
  - 複雑な低消費電力設計の容易化

• 最終製品統合化の変遷。
  - 2000年代: 最終製品の多機能化の波が到来。（例: 血圧計、アルコール検査機、血糖値計測器などをiPhoneに接続可能）
  - 2015年: ポータブルな高機能製品の実現（例: 心肺機能の管理のポータブル化）

• 機能の統合化には階層設計が必須。（ブロック、IPの再利用）
  - CPF1.1は低消費電力デザインの階層設計の容易化を実現。
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Years 2006 - 2009: The Power Format Wars

- Two giants battled with tremendous powers
- But the low power landscape was severely trampled
- Complex issues are never really **Black** and **White**
  - Both formats had their strong and weak points
  - In the end, cooperation was better for everyone
Interoperability with P1801:

Translator Functions
- Name mapping
- Power modes and states
- Power supply sets
- Supply functions
- Rules and strategies

CPF 1.2 File
CPF 1.2 Parser

P1801 File
P1801 Parser

Bidirectional Translator

CPF 1.2 Data Model

P1801 Data Model Compatible Subset

1 A subset of P1801 commands cannot be translated. User guidance will be provided until the ambiguities are resolved.
Cooling Down the Power Format Wars

• **Identify a common Command Set used in both P1801 and CPF**
  - Consistently describe Low Power design intent to drive optimization, verification and implementation
  - Bi-directional translation (CPF 1.2 + design) & (P1801 + design)
  - Resolve ambiguities between the compatible subsets

• **Start to converge the data models of P1801 and CPF 1.2**
  - Complete and release a Open Power Data Model specification
  - Provide guidance for commands outside of translatable subset

• **Focus on the Industry Requirements for the best standard**
  - Improve Block Level IP modeling and representation
  - Build a standard that is better than either P1801 or CPF 1.0
  - Incorporate LPC feedback from CPF 1.0 and CPF 1.1

• **Reach out to P1801 Supporters and work together**
  - Many of the original P1801 supporters adopted CPF
フォーマットの議論の終焉と新たな時代の到来！

- 2006 – 2009年：パワー・フォーマット戦争
  - 過大なエネルギーを費やす2大巨頭の戦い。
  - 最終的に業界のために協業の方向へ。

- P1801 (UPF) との互換性改善
  - CPF 1.2 にてデータ・モデルの共通化を図り、P1801との互換性を向上。
    (一部、共通化の図れないコマンドあり)

- パワー・フォーマット戦争の終焉：P1801陣営との協業スタート。
  - 共通コマンド洗出し。
    - 双方向変換の実現。 (CPF 1.2 ⇔ P1801)
    - 暖昧なコマンドの削減。
  - データ・モデルの共通化。
    - データ・モデル (Open Power Data Model) 策定開始。
    - 共通化できない箇所に対する手引書の提供。
  - 標準化のために業界の要求事項に注目。
    - ブロック・レベル IP モデリングの改善。
    - P1801, CPF 1.0 を超えたスタンダードの策定。
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Industry-wide Adoption of CPF

Silicon Integration Initiative
It was easy to get started in Advanced Low-Power

*A Practical Guide to Low-Power Design*

- **Contents:**
  - Low-power methodology
  - Captures collective effort of 36 Power Forward Initiative members
  - 9 User experience chapters by ARM, ARC, Faraday, Freescale, Fujitsu, NEC Electronics, NXP, Sequence and TSMC
  - 3 new chapters published 12/2008

Free download from:  
[www.powerforward.org](http://www.powerforward.org)  
5000+ Downloads!

Power Aware “Best Practices”
CPF Support Grew a Large Ecosystem

2008 Adoption Aids in the Si2 library:

2009 Adoption Aids in the Si2 library:
Fujitsu Proved it Worked!

Verified with test design

- PSO functional verification with full simulation
- Low power structural and physical check (Shifters/Isolators/Power switches)
- Domain aware place and route

Conclusion

- Functional verification is necessary for complex PSO design for design bugs
- Structural check with CPF could verify LP design
- Fujitsu supports CPF-based ASIC flow for their customers

Silicon Proven in September 2007
低消費電力設計指針の標準としてのCPFの現状

- 業界内で数多くの企業がCPFを採用。
- Power Forward Initiative (PFI) より低消費電力設計ガイドを2008年4月にリリース。これまで5000以上のダウンロード。
  - 日本語翻訳版を2008年11月にリリース。これまで、約300のダウンロード。（日本ケイデンスのWebsiteからダウンロード可能）
- CPFの実用に向けて数多くの手引書を発刊。（Si2のWebsiteからダウンロード可能）
- 数多くの品種がCPFを使ってテープアウト。（例：富士通様では自社製品、及びASICに適用済み）
### What’s in Your Future?

<table>
<thead>
<tr>
<th><strong>CPF Evolution</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete <strong>CPF 1.2</strong> Enhancement List</td>
</tr>
<tr>
<td>Complete and release the <strong>Open Power Data Model</strong> specification</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>CPF Support</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete all support materials for the <strong>CPF 1.1 Enhancements</strong></td>
</tr>
<tr>
<td>Begin Support for CPF 1.2 in 3Q - 4Q/2009</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>CPF Related Events:</strong></th>
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</thead>
<tbody>
<tr>
<td>Low Power Seminar</td>
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<tr>
<td>Design Automation Conference:</td>
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<tr>
<td>EDS Fair</td>
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</table>
Conclusions from the Year 2015

- **CPF was established as the Gold Standard low power format**
  - Adopted world-wide by EDA companies and by 100+ design teams
  - Proven record of success based on first time silicon at Speed & Power

- **CPF evolved as a industry standard driven by the real life requirements from key stake-holders in the LPC**
  - CPF 1.0, CPF 1.1 and CPF 1.2 Enhancement Roadmaps were clearly defined and achieved their target release dates

- **Si2 helped Low Power to become the New Currency**
  - Wiki-based collaborative standards for Low Power Design Web-enabled adoption support for Europe, Asia and United States
  - Rich collection of Low Power adoption aids
  - Multiple Si2-sponsored Low Power events

*Innovation Through Collaboration*
本当にありがとう
Si2 Contacts

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