ePIXfab full training – November 2013 – Leuven (B)

Silicon photonics design flow: state of the art

Pieter Dumon and Twan Korthorst

Creating a Photonic Ecosystem

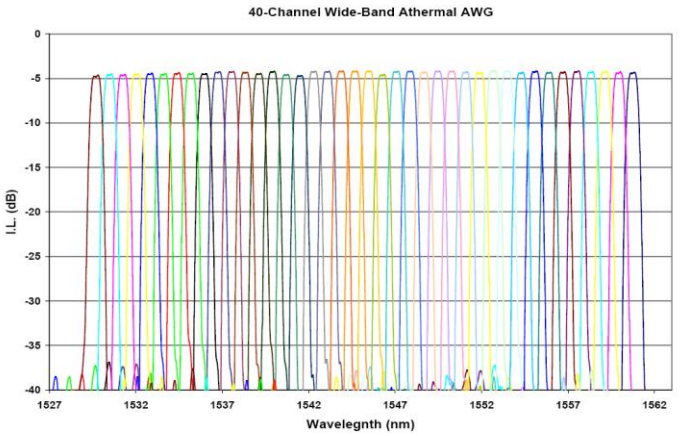
- Several programs in Europe (since 2005)
  - Such as Epixnet, EuroPIC, Helios, Essential and now **Plat4m**
- Bring together all players
  - Fabs, design houses, packaging, software providers, end users
- Create eco-system equivalent to electronics industry
  - Have fabs open up and document processes and building blocks
  - **Define standards and improve Photonics Design Automation**
  - Create MPW shuttle organizations (like *ePIXfab*)

Photonics Design Automation

- Photonics ≠ CMOS electronics
  - <1% of processed wafers in CMOS
  - Typical linewidth sizes: 0.15 - 4 micron
  - Current process tolerances high
  - "RF-like" or "analogue" behaviour

    → *Telecom C-band is 1530–1565nm = ~193 THz*

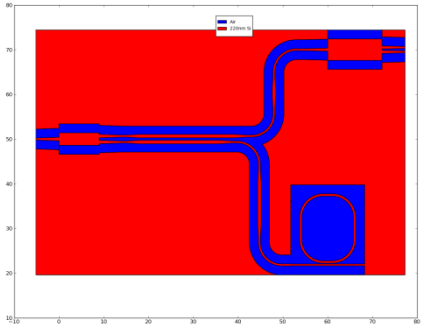
40 channel integrated optical multiplexer with a channel spacing of 100 GHz for telecom applications.

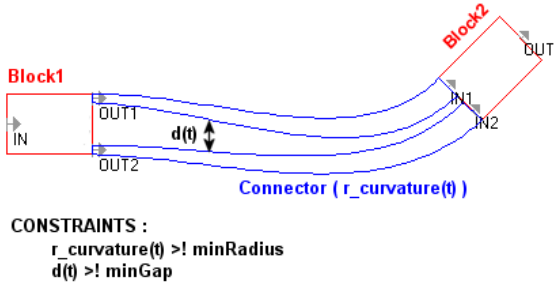


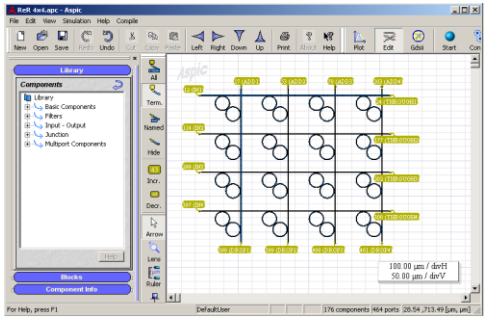
Picture and spectrum are courtesy of the Kaiam Corporation.

Photonics Design Automation

- Photonics ≠ CMOS electronics
  - "RF-like" or "analogue" behaviour requires:
    - → *Smart simulation tools*
    - → *Accurate and flexible definition of shapes (all angle)*
    - → *Control of phase (differences)*
    - → *Connectivity and "smart" routing routines*
    - → *Libraries with parametric building blocks*







Integrated Optics and Photonics

- Various material systems and technologies
  - Si / SOI
  - InP / III-V materials
  - TriPleX and other SiO2/Si3N4 technologies
  - Polymers
  - …
- With their mass and niche market (potential)
  - Telecom
  - Datacom
  - Sensing
  - Microwave photonics
  - …

Focus: Silicon Photonics

- Silicon fabs are using EDA tools
  - Especially for DRC, sign-off and tape-out
- Photonics designers and non-silicon fabs are using PDA tools
- EDA tools are –not directly– suitable
  - All angle designs, shape definition, simulations, DRC
- PDA tools require additional capabilities
  - Mature DRC, auto-routing, LVS, ORC, RET

Focus: Silicon Photonics

- Collaborative project: Photonic Libraries and Technology for Manufacturing (Plat4M)
  - 15 partners, led by CEA-Leti (Fr.)
  - Make silicon photonics ready for transition to industry
  - From elementary building blocks to real photonic circuits
  - Streamline and consolidate the design flow

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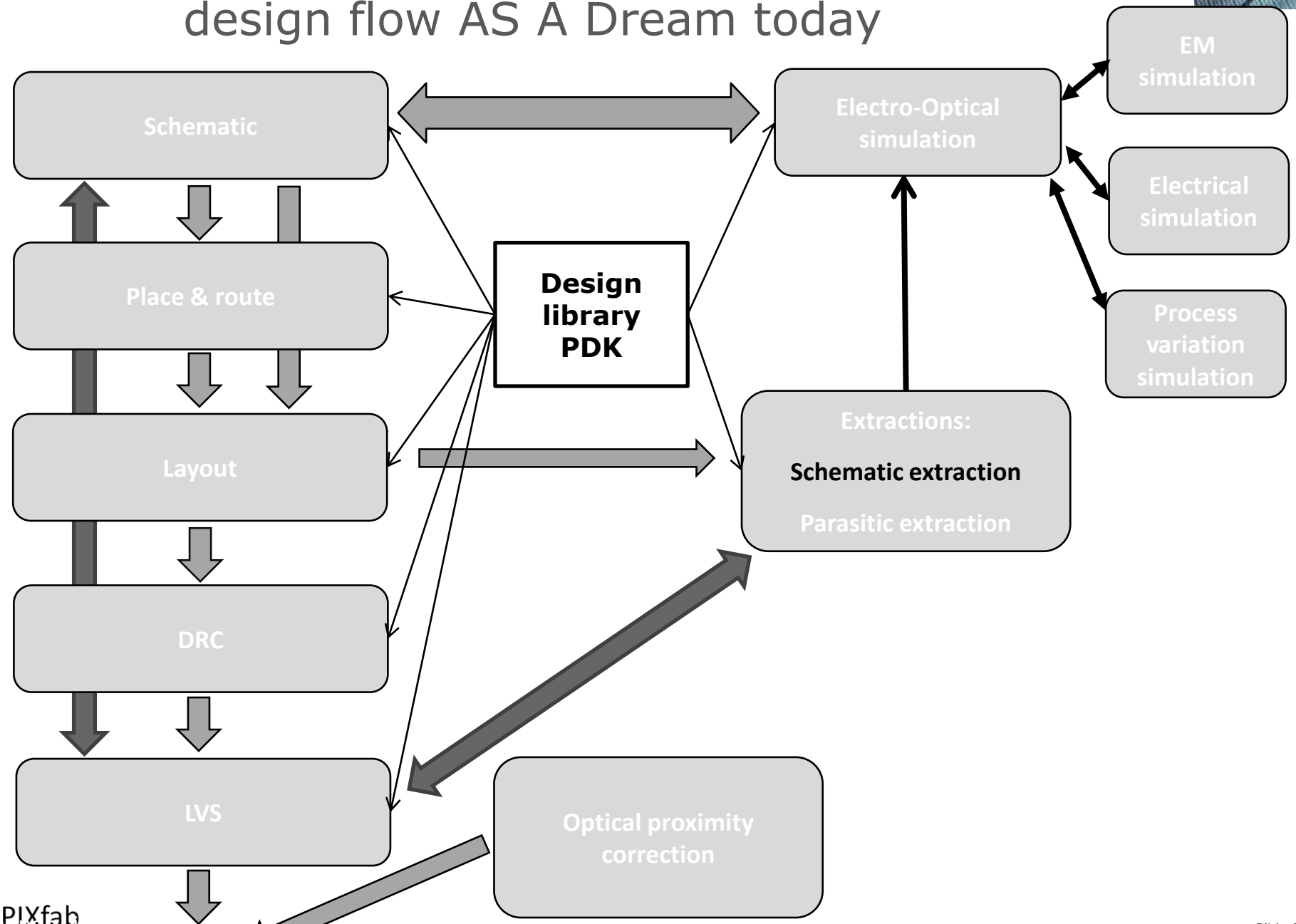
  - **Streamline and consolidate the design flow**

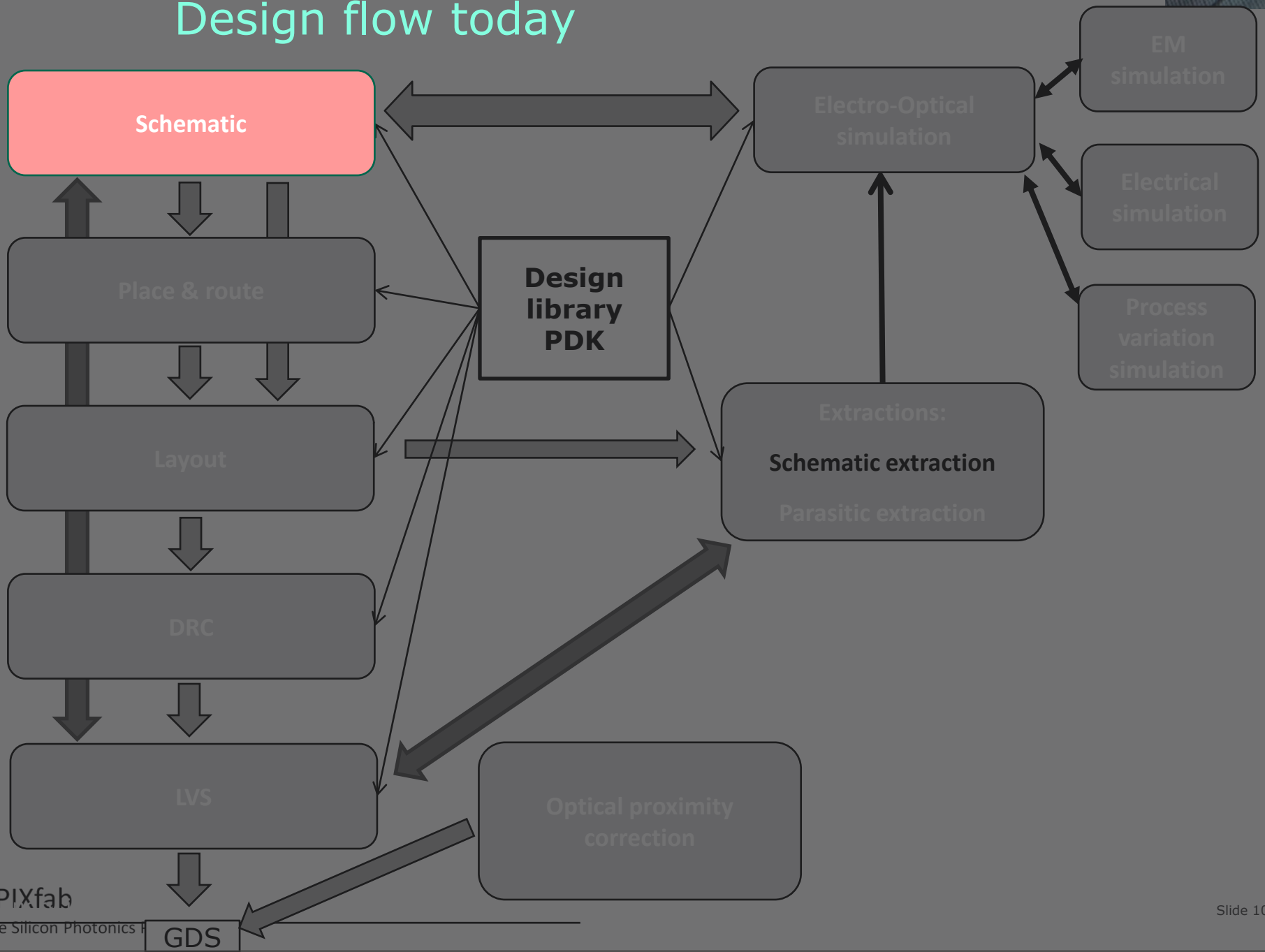
First step: investigation of current **working practices** and **tools** in the consortium and define the ***ideal*** **design flow**

Second step: identify the current **state of the art**

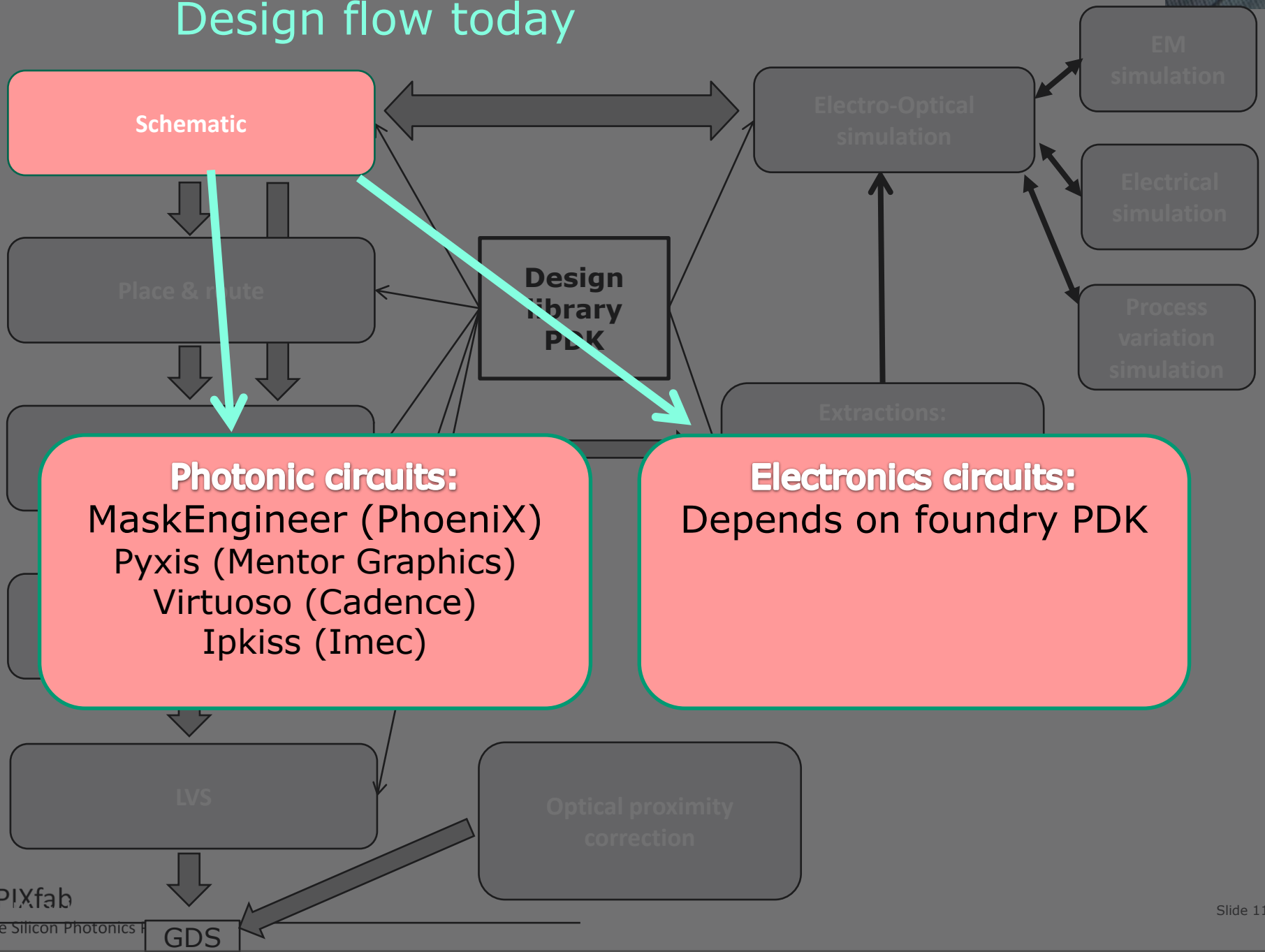
design flow AS A Dream today



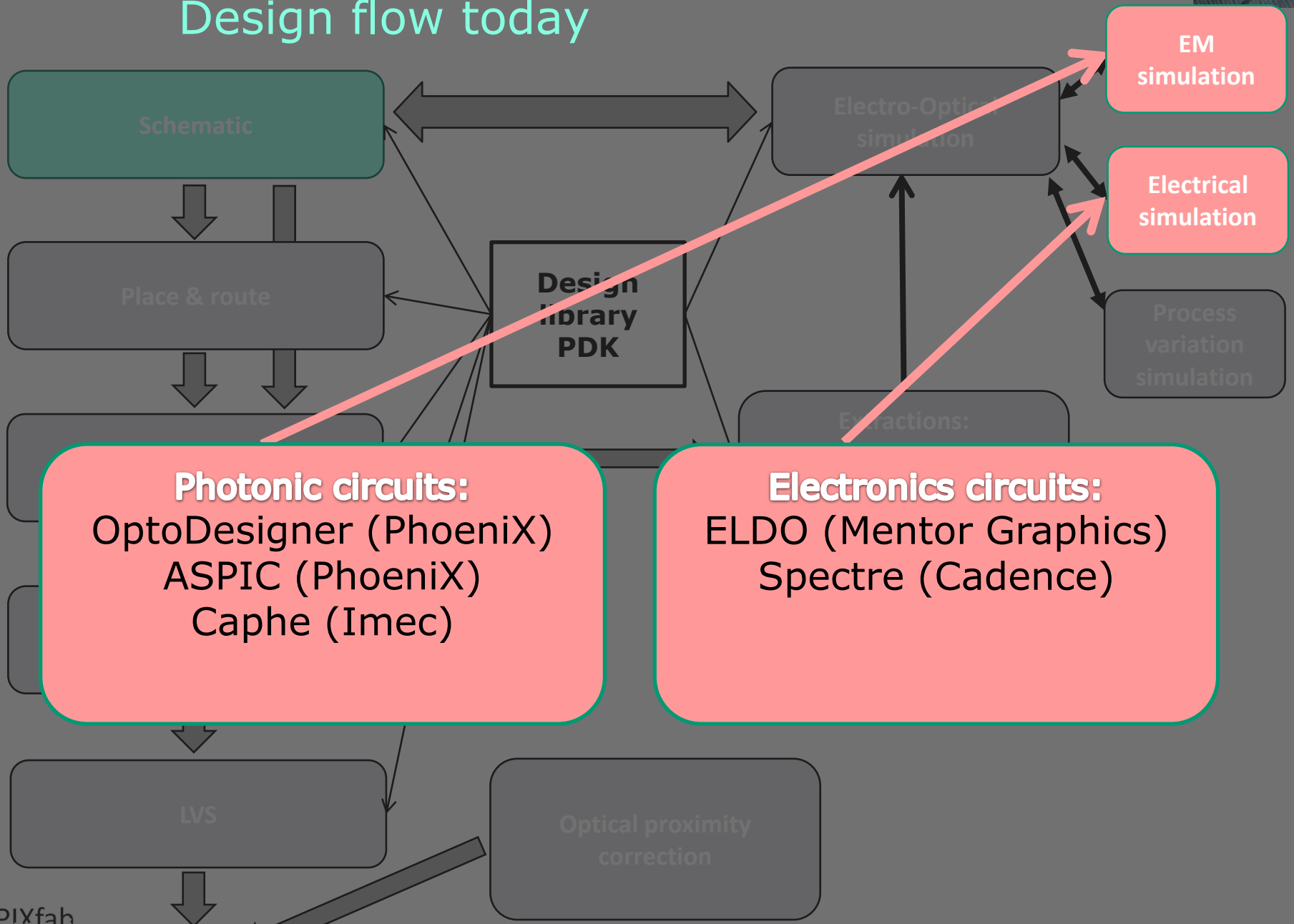
Design flow today



Design flow today



Design flow today



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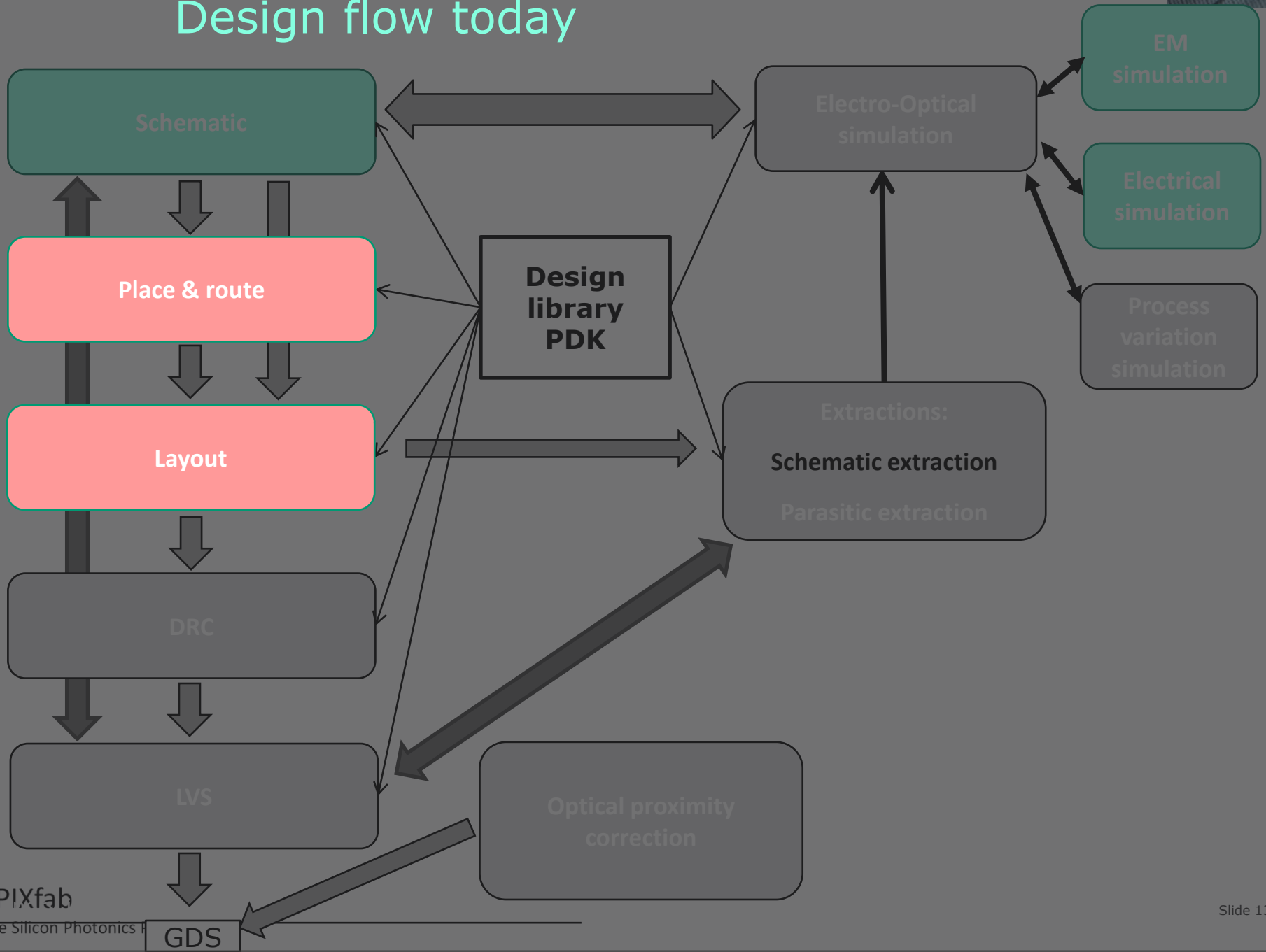

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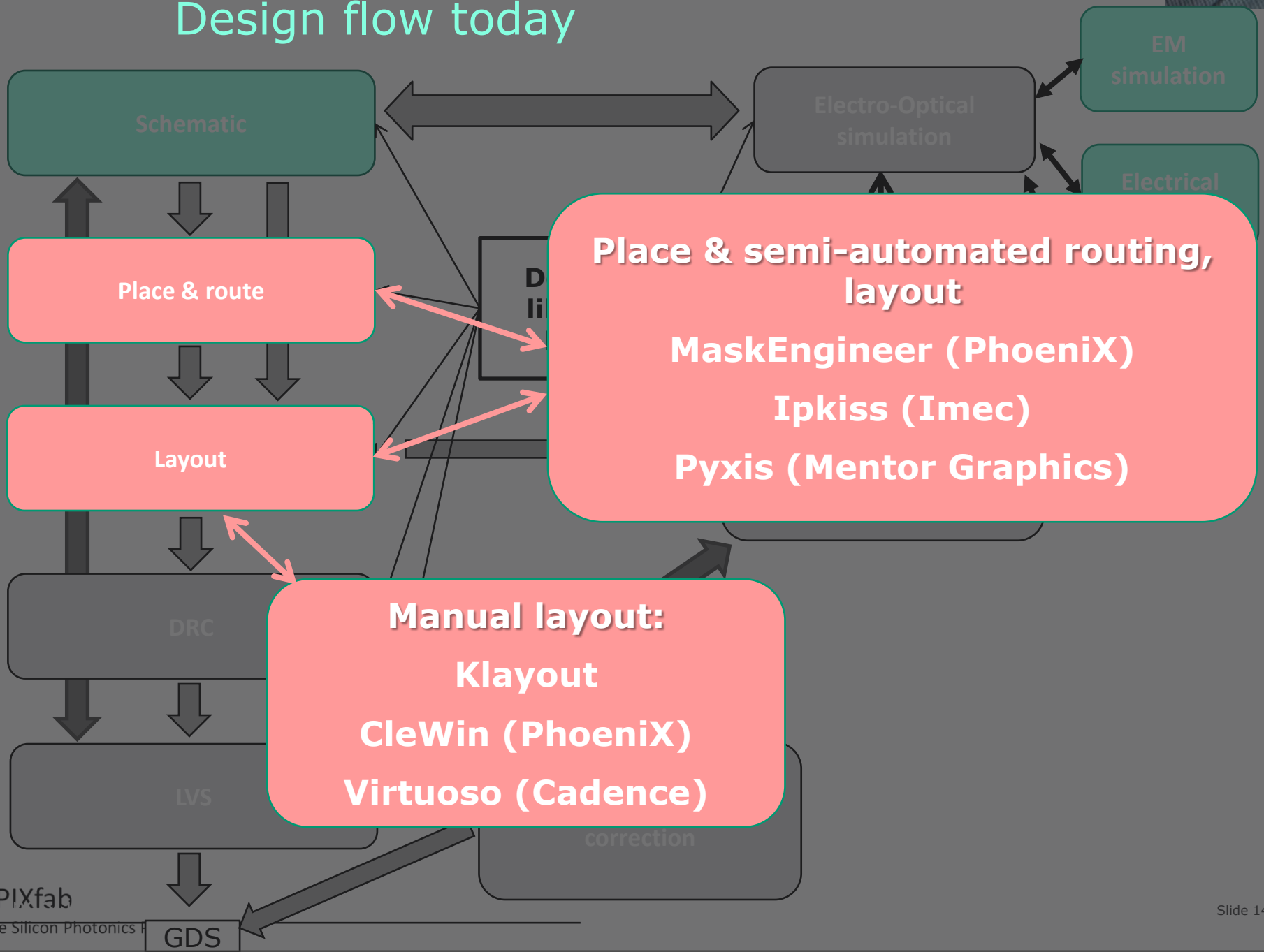

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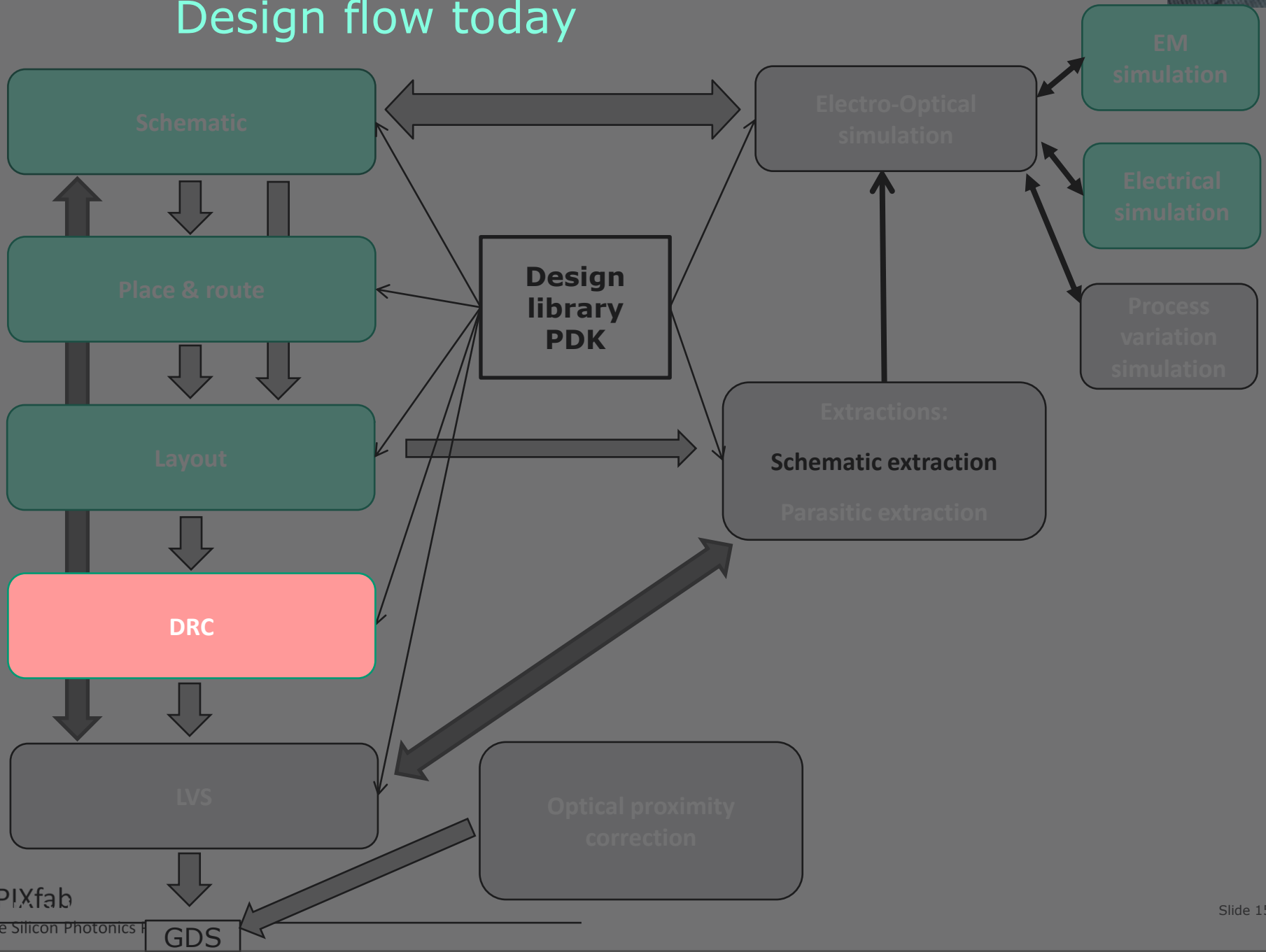

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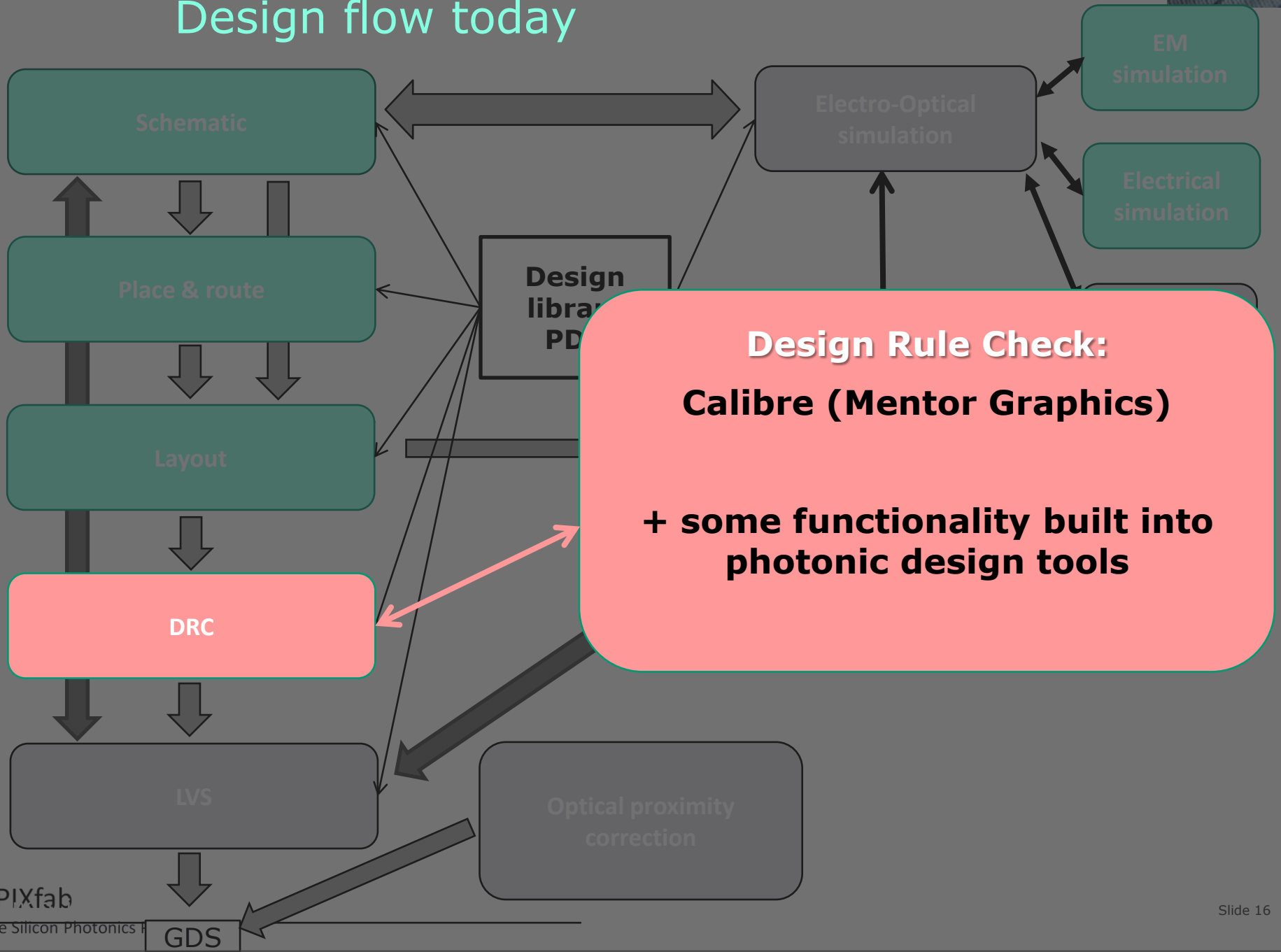
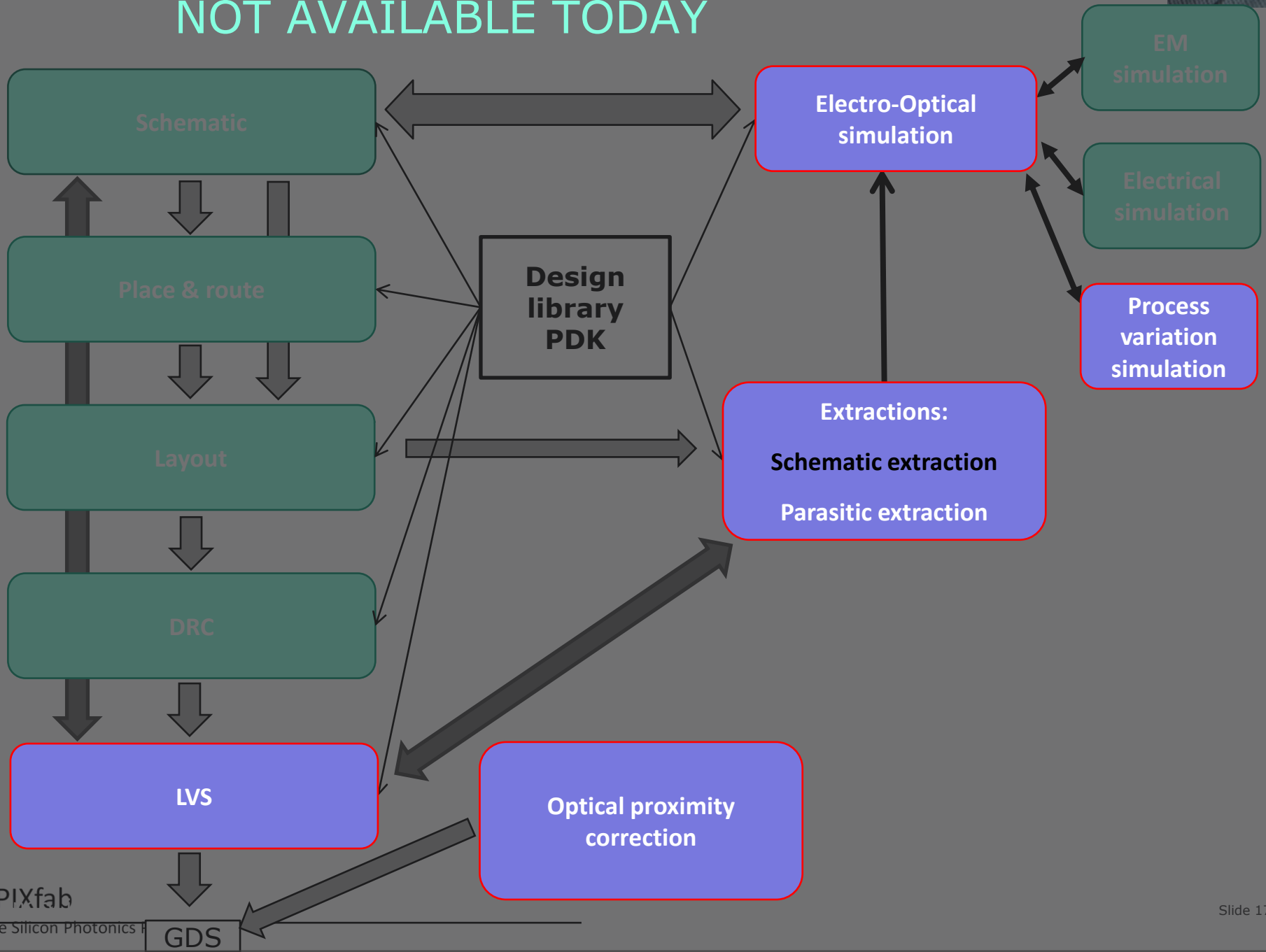


NOT AVAILABLE TODAY



Collaboration and Standardisation

- Collaborative project: Photonic Libraries and Technology for Manufacturing (Plat4M)
  - 15 partners, led by CEA-Leti (Fr.)
  - Make silicon photonics ready for transition to industry
  - From elementary building blocks to real photonic circuits
  - **Streamline and consolidate the design flow**
- EDA interaction through Si2 and Mentor Graphics
  - Extend OpenAccess to accommodate photonics (SP-TAB)
  - Improve EDA tools
  - Integrate PDA and EDA

Collaboration and Standardisation

Mentor Graphics: improve EDA capabilities

- Layout generation and editing with the **Pyxis** tool suite
- Physical verification with the **Calibre** tool suite
- SPICE simulation with the **Eldo** tool suite

Collaboration and Standardisation

IMEC: support EDA and PDA improvements

- Design kit integration for IMEC technology
- DRC and LVS using Mentor Graphics Calibre
- Device models
- Variability modeling in the design flow

Collaboration and Standardisation

PhoeniX Software

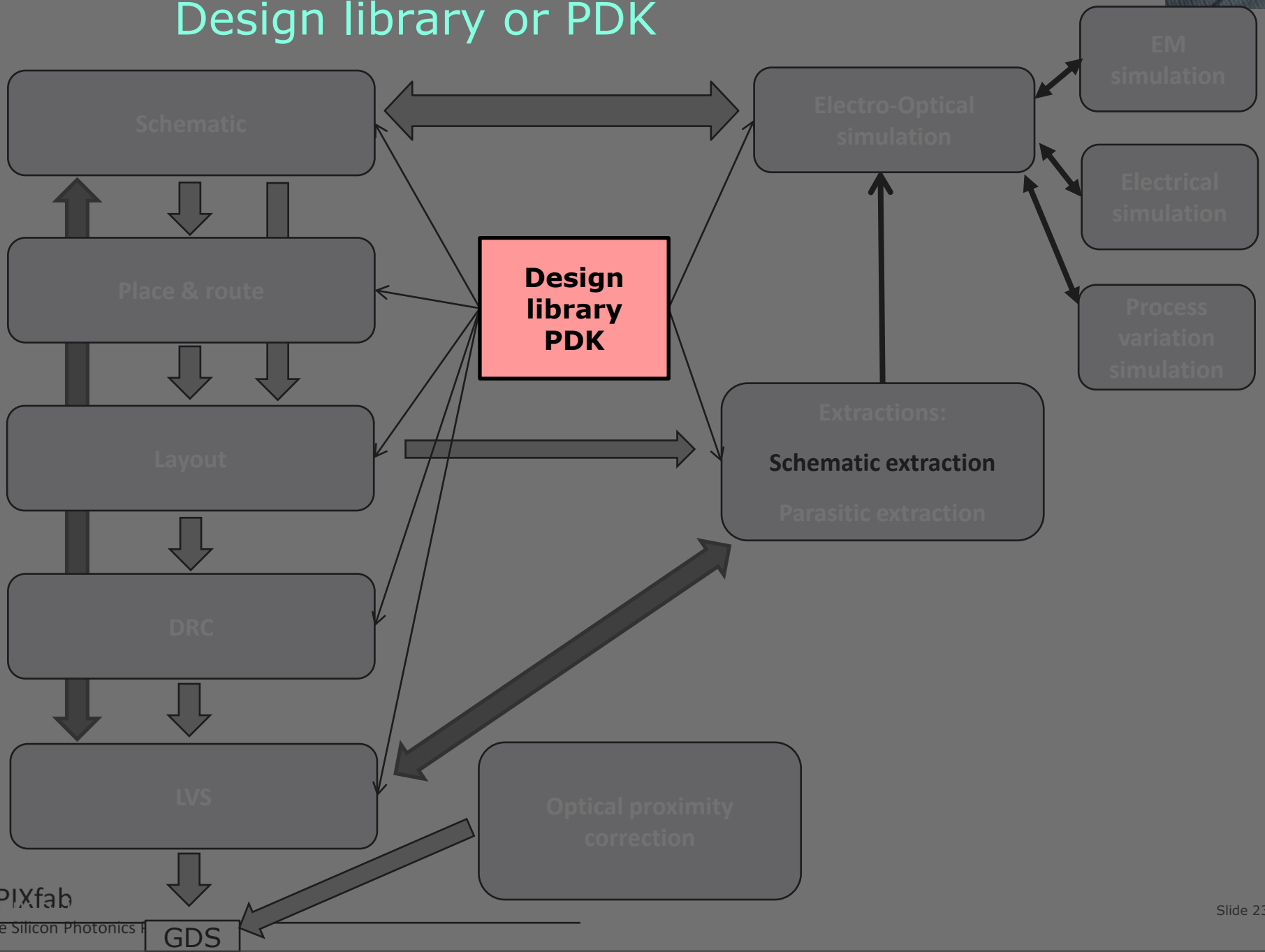
- Improve photonics design automation (PDA) and electronics design automation (EDA) integration
- Layout generation of photonics building blocks with **MaskEngineer** and **OptoDesigner** for integration in EDA tools

Collaboration and Standardisation

Si2: SP-TAB

- Open for all interested parties
- Extend **OpenAccess** to enable co-design of electronics and photonics
- Si2 provides manpower to architect, implement and document the extensions
- Members provide critical domain knowledge about photonics design data and flows, test code, and provide feedback

Design library or PDK



What is a PDK?

A Process Design Kit is a common software tool in micro-electronics

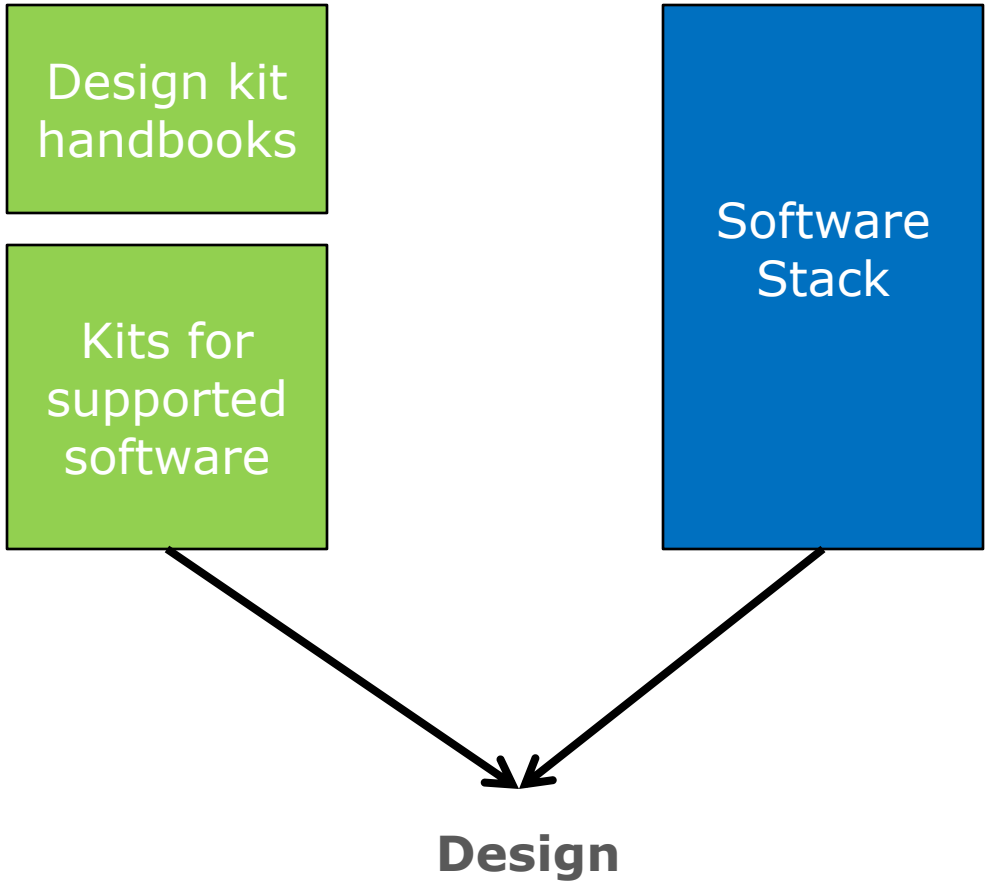
- Fab dependent *fixed* technology
- Library with *validated* cells
- *Reduced* design freedom
- *Guaranteed* functionality

- Design validation (DRC, LVS)
- Integrated functional simulations

What does a PDK look like?

- Design rule manual, technology handbooks, …
- Library of validated Building Blocks
  - Layout and process information
  - Design and verification rules
  - Measurement data
  - Models
  - Simulation settings
  - IP information
- Chip and Packaging Templates
  - Die sizes
  - Optical, DC and RF port locations

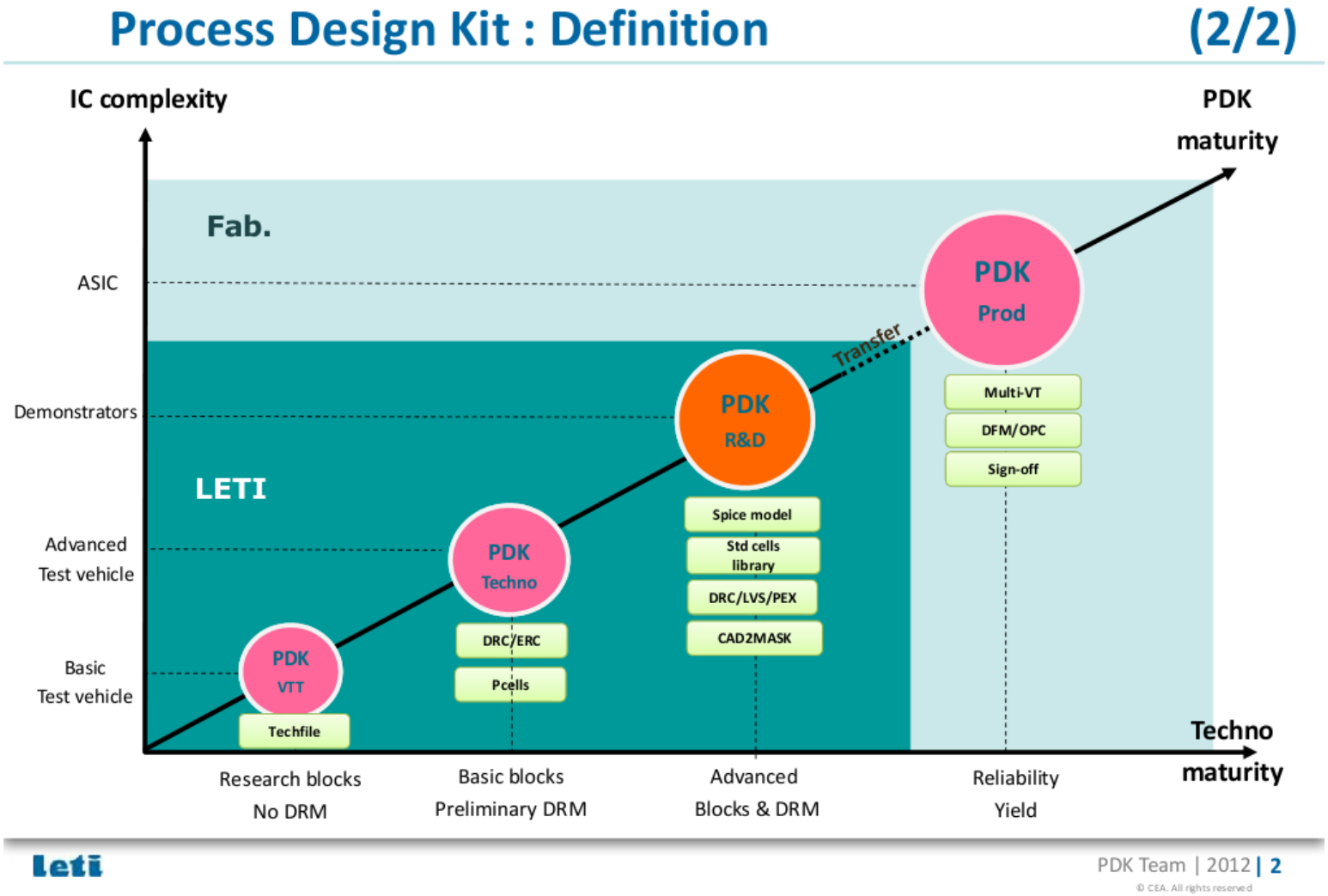
What does a PDK look like?



Present Status of PDKs

- PDKs are specific for a foundry
  - Silicon Photonics PDKs are currently available for:
    - imec (passive and active platforms)
    - CEA-Leti (passive and active platforms)
    - IHP
    - VTT
    - OpSIS/IME
- Foundry has control over release PDK
  - Typically made available through MPW shuttle organization like ePIXfab, Europractice, OpSIS, MOSIS, CMC
  - Requires signed NDA and/or DKLA

Present Status of PDKs



Present Status of PDKs

		Silicon Photonics				
		ePIXfab / Europractice / Mosis / CMC				OpSIS
		imec	CEA-Leti	IHP	VTT	IME
	PDK maturity level	**III**	**I / (II)**	**I**	**II**	**III**
	Mask layout and technology set-up files	+	+	+	+	+
	Material and process information for physical simulations	+	+	+	+	+
	Models and/or measurement data for circuit simulations	-	-	-	-	+/-
	Number of building blocks	~20	<10	0	~10	~40
	Design rules	+	+	-	-	+
Lumerical	Interconnect					x
PhoeniX Software	MaskEngineer/OptoDesigner/FieldDesigner	x	x	x	x	run 5
Mentor Graphics	Pyxis	planned				x
	Calibre	x	x			x
University of Gent	Ipkiss framework	x			x	

Thank you

www.epixfab.eu