Developing vision for RLC parasitics framework on OpenAccess

Si2 OpenAccess Parasitics Work Group

Outline

- Interconnect modeling challenges
- Example techniques to address these challenges
- OpenAccess as a Platform to enable these techniques
- What *CAN* be done:

  OpenAccess Parasitic Infrastructure Vision
- What does the industry *WANT*:

  Challenge all to help shape the vision and set priorities by responding to the OA Parasitic Work Group Survey

Interconnect modeling challenges at low geometries

- **Design size and complexity increase**
  - More functionality put on the die thanks to process scaling
- **Wire resistance scaling**
  - Significant increase of wire sheet resistance at low process nodes
  - Wire delays becoming increasingly important – an increased FET Id_{sat} no longer guarantees higher design performance
- **Lithography, etch and CMP effects**
  - Increased complexity of R and C modeling and estimation
  - Increased and more complex role of neighboring wires and wire density
- **Variability (of wires AND transistors), lower VDD-Vt, etc.**

Design flow implications

- **Need more accurate wire modeling earlier in the design flow**
- **Need to extract wire parasitics at more design corners**
  - Worst/Best C, Worst/Best RC, FET Temperature inversion, etc.
- **Longer extraction times and larger netlist sizes**
- **Longer simulation times**
- **Slower turnaround time of optimization and analysis loop**

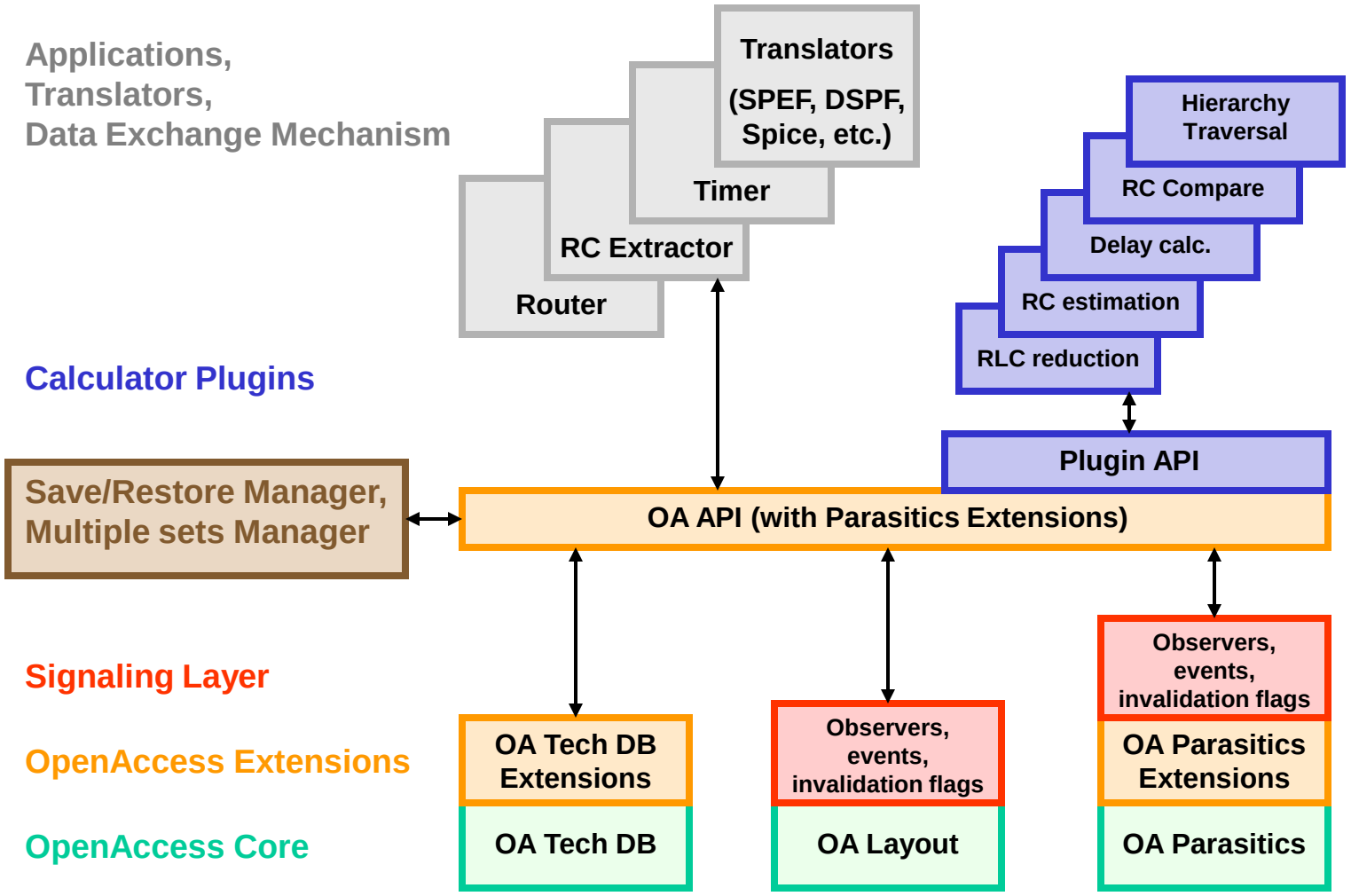
Extraction techniques to address the challenges

- **Incremental extraction**
  - Only extract those nets that changed or are influenced by a change
- **Extraction and netlisting accuracy control at finer granularity level**
  - Less critical nets can be extracted or netlisted at lower accuracy
- **Improved RC reduction effectiveness**
- **ECO optimization loop enablement**
  - Integration with route and analysis tools
  - Not just in the regular place & route flows but also for more specialized use cases (clock optimizations, custom design, etc.)
- **Hierarchical extraction**
  - Enable simulation of various sub-circuits at different accuracy and abstraction level
- **Please provide feedback in the survey about your specific needs**

OpenAccess as a platform to enable these techniques

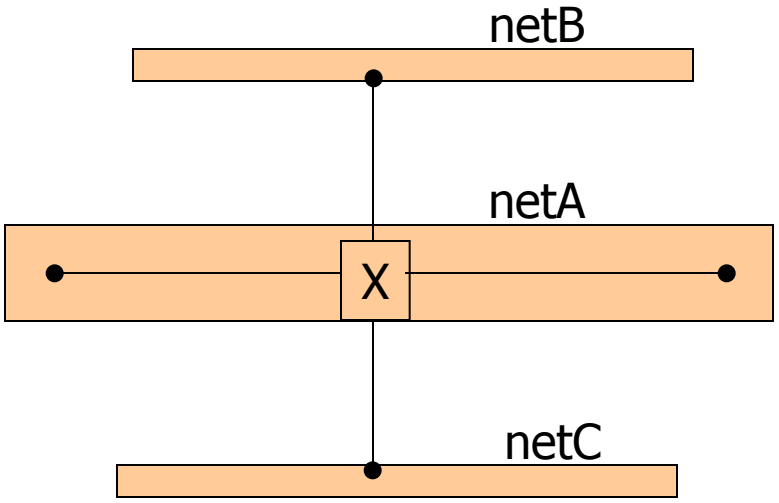
- **Well established in the industry**
  - The backbone of custom design entry flows
  - Used in large number of other tools
  - Proven set of importers and exporters
  - Open API, well defined contribution process for extensions
- **Includes solid foundation for RLC parasitic representation**
  - On-demand load/unload of parasitic networks
  - Solid support for coupling capacitors, self- and mutual-inductors
  - Ability to use multiple Analysis Operating Points for multi-corner support, as well as multiple parasitic networks on the same net
  - Association between parasitic subnets and layout route segments or shapes
  - Supported both in block and occurrence domains
  - Data structures for detailed as well as reduced views
  - Basic SPEF-in and SPEF-out translators
- **Extensibility and cooperative processing features make it a suitable platform for building parasitic infrastructure**
  - Application extension mechanism (appDefs)
  - Plug-in mechanism
  - Observers (to enable event driven flow)

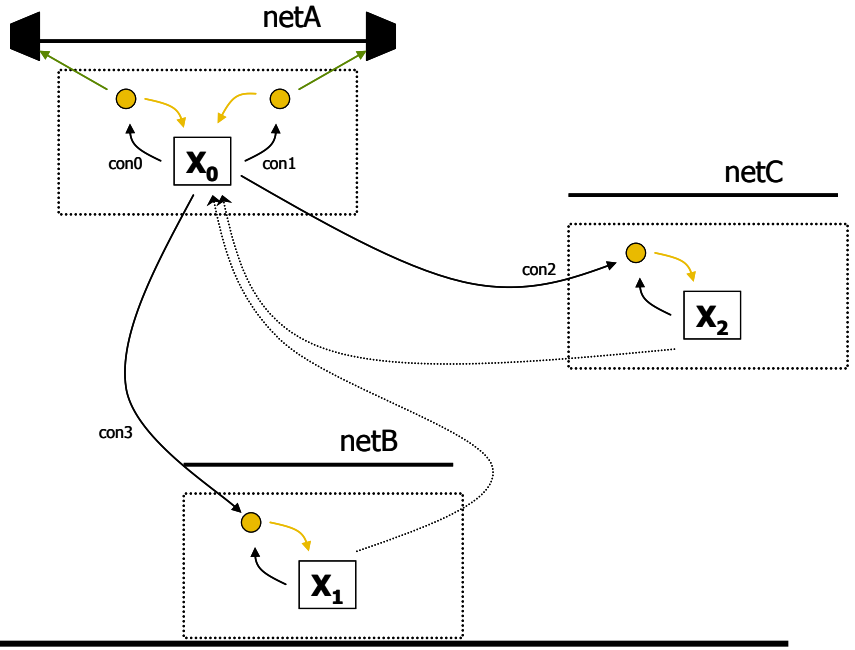
OpenAccess Parasitic Infrastructure Vision Diagram



Extension to support arbitrary parasitic devices

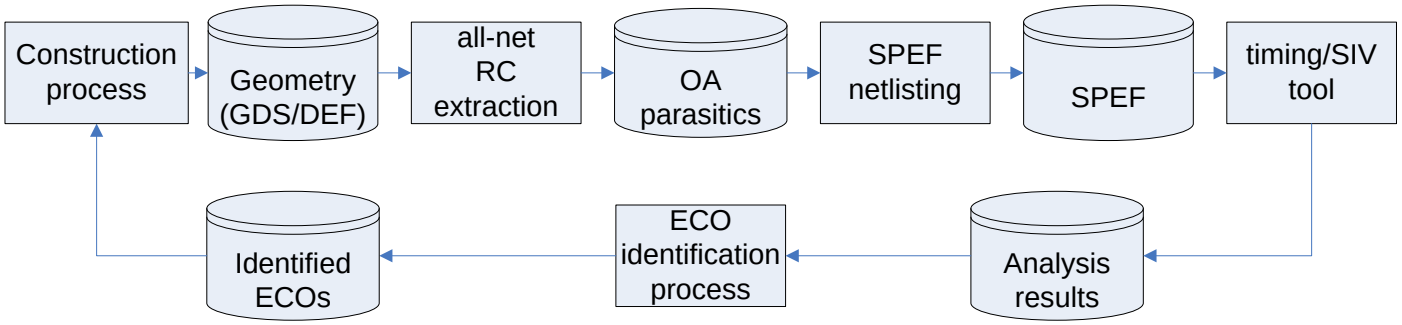
- **Donated by Tektronix in 2008**
- **Extents OA Parasitic Model to support parasitic devices with arbitrary number of connections, model name, and a set of parameter / value pairs**
  - Makes the model more suitable for analog and RF applications
  - Initially, the model has been more SPEF-like and tailored mostly for digital designs



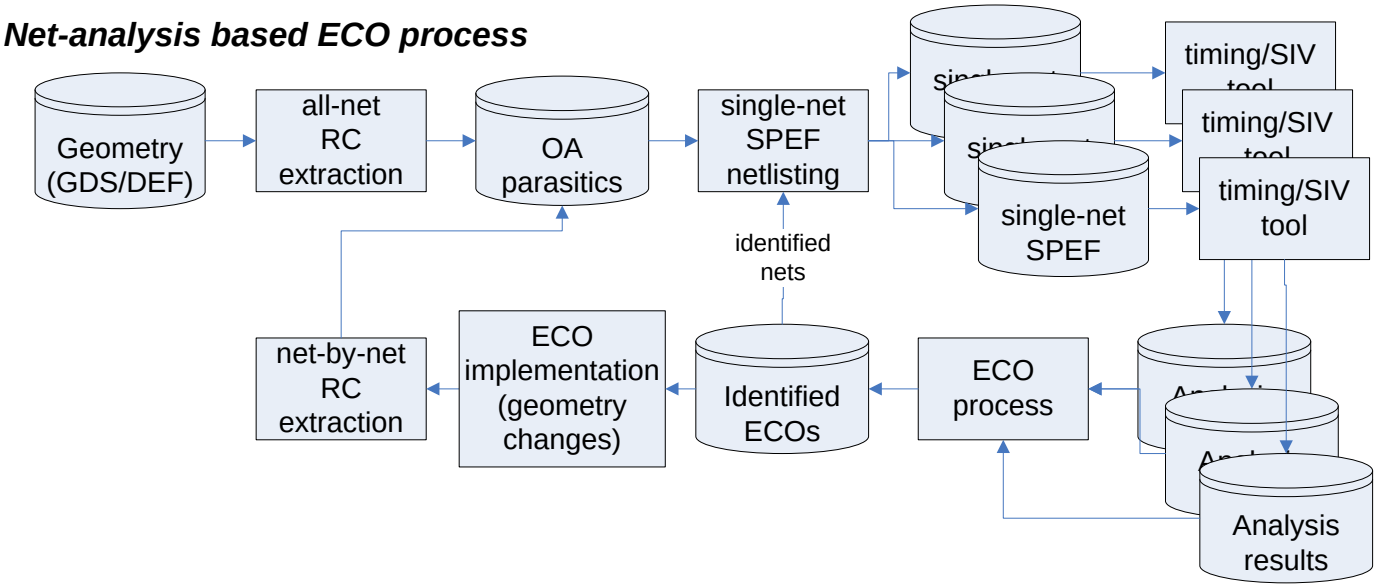


Incremental Extraction and Analysis Flow

Present OA extraction / ECO model



Net-analysis based ECO process



Incremental flow use case

Why would an ASIC design team benefit from an incremental RLC extraction flow?

- Because industry standard tools have gaps in areas specific to high performance design
- Example: Chip level clock distribution optimization
  - *The clock distribution can have special features not handled well by off-the-shelf place & route CTS algorithms: differential pairs, parallel drivers, etc.*
- Goal: Optimize buffer placement and route for minimum clock uncertainty.
- Assumptions:
  - *Semi-automated or manual Buffer placement*
  - *Automated Route*
  - *Spice based Delay calculation*
- Four applications involved:
  - *Design application (for Buffer placement)*
  - *Router*
  - *RC Extractor*
  - *Spice simulator*
- Problem statement: conventional flow has too slow turnaround time for buffer placement optimization after design changes

Other possible priorities

- **Hierarchical stitching**
- **Extension to support Parametric SPEF**

However, it is up to YOU to decide on the next priorities

by responding to OA Parasitic Work Group Survey

OA Parasitic Work Group Survey

1. **What RLC extraction capabilities are you missing in EDA vendor solutions?**
2. **What RLC parasitic infrastructure are you currently using?**
   - SPEF / DSPF
   - OpenAccess parasitic view
   - Other industry standard (or EDA vendor proprietary) views
   - in-house database view
3. **Have you used OpenAccess parasitic model? Select one item:**
   - Did not see a need to look into OA parasitic view yet
   - Looked at OA parasitic view but found it deficient (Deficiencies?)
   - Looked at it, liked it, but not yet moved to it (Barriers?)
   - Actively using OA parasitic view (How is it useful?):
4. **If the OA Parasitic Model supported items listed in #1, would you be more likely to move to it ?**
5. **Would you be willing to help out in the OA Parasitic Work group to come out with specifications for these capabilities ?**

OA Parasitic Work Group Survey (Cont.)

Please download the survey from the following Web site:

http://www.si2.org/?page=1280

Thank You !

Backup: Incremental flow example implementation