Si2 Newsletter

Fall - 2011

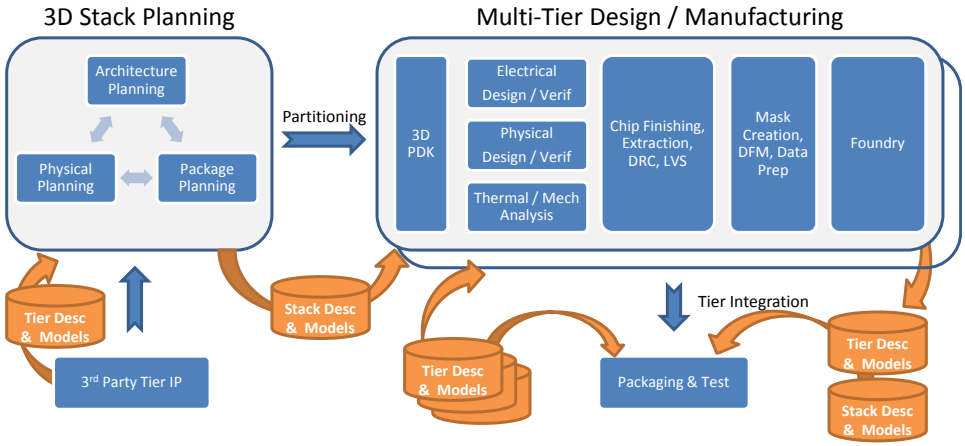
Open3D TAB Kicks Off

Working Groups Formed

The Open3D TAB has begun regular meetings in parallel with the on-going effort to gather critical mass in membership. At a recent meeting where 18 representatives from 14 companies attended, it was agreed that the most urgent needs in the area of standards were in the 3 topics below:

• Definition of the power distribution network across the tiers of the 3D stack, a topic for which a contribution has already been received in response to the request for technology (RFT) that was released earlier in the year

Open3D - Target Areas for Standards



• Means to enable thermal design of the entire 3D stack including, for instance, expressing thermal constraints between neighboring dies

• Expressing design constraints into and out of the path-finding and floorplanning stage of the overall design process

An additional topic – creating a dictionary of terms – was also discussed and it was agreed that this task would be distributed to the different working groups that would tackle the above 3 focus areas and the resultant documents would then be merged into a single dictionary. These working groups are now being populated by representatives of member companies.

A final topic discussed at this meeting covered the areas of design for test (DFT) and automatic test pattern generation (ATPG). This was deferred to the currently on-going effort under the IEEE.

16th Si2 Conference

This conference will cover the increasingly inter-related areas of OpenAccess, Design for Manufacturability (DFM), Low Power design, and Open PDK standards. Updates on the ongoing enhancements to OpenAccess and it industry adoption will be presented along with status and plans for the future for all coalitions and projects. Speakers will include participants from: AMD, Cadence, Calypto, Entasys, GLOBALFOUNDRIES, IBM, LSI, Mentor Graphics, SpringSoft, STMicroelectronics, and TI. More info at: http://www.si2.org/?page=1384

Dr. Ajoy Bose, Chairman, President, and CEO of Atrenta will provide the keynote address, entitled “SoC Realization – Building a Bridge to New Markets and Renewed Growth”.

There will be a DFM session covering the latest status of the projects in the DFM Coalition, such as, standardization of a format to transfer parasitic data from a foundry or technology provider, as well as the approach taken to verify the standards created by this coalition. There will also be a presentation on DRC+ from GLOBALFOUNDRIES. Another session will cover the progress made in the past year in defining standards for open PDK’s which are the fundamental building block for semiconductor design. The OpenAccess community has grown dramatically and the standard is now a "must have" for industry players. The OpenAccess sessions will highlight relevant experiences and new developments. Low Power Coalition work in power modeling standards, and application of the latest standard will be presented, including major contributions that the LPC has made to enhance the IEEE1801 standard.

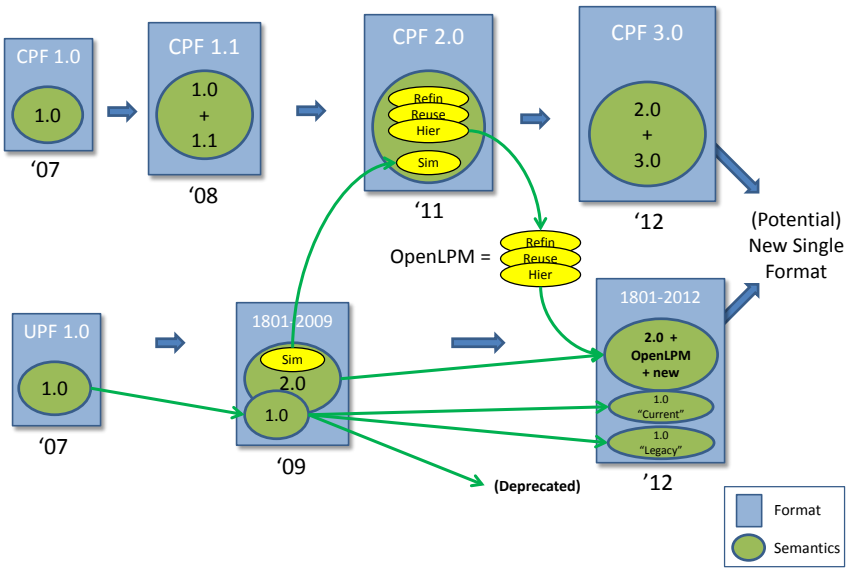
As in prior conferences, there will be an evening session that will showcase demos of advances based on the technologies offered by Si2. This session will also serve as a valuable opportunity for networking. Refreshments will be served.

To register on-line: https://www.si2.org/openeda.si2.org/si2_store/#c1 or a fax/mail form: http://www.si2.org/?page=1254. Breakfast, lunch and a reception are included in the registration price. The lunch is sponsored by Cadence Design Systems, and the Demo/Networking Reception by NanGate.

Open Low Power Methodology

Bridging the Gap Between Power Formats

The Path Towards a Single Power Format



In February, the Low Power Coalition (LPC) published their third release of the Common Power Format standard, with over 100 pages of (backward-compatible) enhanced capabilities including added CPF commands to enable greater compatibility with IEEE 1801. The LPC also created the CPF/UPF Interoperability Guide to relate commands in CPF and equivalent mapping to 1801-2009. Yet there are limitations to what can be mapped, notably with the older UPF 1.0 constructs.

Many industry-leading companies spanning fabless, IDM, IP, OEM, and EDA have underscored to Si2 the ongoing negative impact on productivity when trying to work with both CPF and UPF/1801-2009 in tool flows, despite best-effort command mapping. The root of the problem is deeper than syntax differences – it is about incompatible methodologies for how to organize and manage low power intent data. This became clear after recent customer visits in the U.S., Asia, and Europe, so Si2 chose to offer our help and leadership in resolving those gaps with a coordinated effort being called "OpenLPM" (LPM = Low Power Methodology).

OpenLPM is not a new standard or new project - it is a proactive approach by Si2 and our LPC members to resolve these productivity challenges by contributing certain CPF technology to the P1801 Working Group (WG). This allows the P1801 WG to enhance the capabilities and use cases (methodologies) in the 1801 specification for a smoother overall flow when working with both environments. Three primary features are required for a converged low-power methodology:

(a) Power-domain-centric organization of intent;
(b) Successive refinement of power intent detail; and
(c) Formal support of hierarchy for IP reuse.

In May, Si2 and the LPC made a technology contribution of these features from CPF to the P1801 WG. It is Si2's sincere hope that these will not only be helpful to improve the next revision of 1801 (targeted for 2012), but will also make major inroads in reducing the friction in working with multi-vendor tool flows. The next step will be for the P1801 WG to determine which portions of the Si2 contribution (if any) to accept for incorporation into the next revision of 1801. Si2 has been an active member of the P1801 WG and will continue to support the LPC charter to lead in low-power flows, independent of format. In addition, the LPC is updating the interoperability guide, located at http://www.si2.org/?page=1201, to reflect the advances in Low Power Design contained in CPF 2.0. This upgrade to the interoperability guide will follow the same format as the previous version in denoting commands that are identical, commands that are similar but require care in using, and commands that are incompatible. As the LPC and P1801 move forward, attention is being given to reducing the number of incompatible commands.

A press release explaining additional details of OpenLPM can be found at: http://www.si2.org/?page=1348

Low Power Modeling Progress

While the Format activities are moving forward in the LPC, there is a parallel effort in Open Low Power Modeling to enhance the ability to allow more accurate power analysis at the system level. A key element is to analyze larger and larger blocks by reducing greatly the compute resources necessary for accurate simulation of large blocks through an advanced power contributor modeling and analysis approach. This work has been developed over the last three years by the LPC and represents a major step forward in characterization, modeling, and simulation efficiencies.

Currently, existing models directly model energy and power as outputs, the modeling approach being proposed model the contributors to power separately to allow PVT indepence, correct statistical behavior, ease of characterization and much greater simulation efficiency. This approach using advanced contributor models will be presented at the 16th Si2 conference on October 20, 2011.

OpenDFM

The OpenDFM specification describes a high level, EDA tool independent meta-language to check for a variety of Design for Manufacturability (DFM) problems. OpenDFM rules can be directly translated from the OpenDFM meta-language into the native verification languages of different DRC engines with no loss of accuracy or performance.

OpenDFM does not describe the implementation of design rule checks; it only describes the patterns to be verified. The full capabilities of the underlying DRC engine that executes the rule, in its native language, can be used during implementation. The goal of the OpenDFM is the promotion of a standard format to describe the patterns and parameters required to analyze and repair DFM hotspots. The OpenDFM specification does not describe the models or the algorithms used for rule implementation. The primary objective of the OpenDFM format is to provide excellent clarity of the physical verification intent for problematic IC layout patterns.

Different implementations of an OpenDFM rule are checked via a comparison with the expected result pattern that is provided for each rule. When a native rule implementation is XOR clean with the expected result pattern for that rule then the implementation is considered qualified. It is absolutely not the intent of OpenDFM to constrain the implementation of OpenDFM rules to a common subset of DRC engine features. Such an approach would lead to a Lowest Common Denominator of implementation capabilities. OpenDFM encourages each engine to maximize whatever features, performance or accuracy it can achieve.

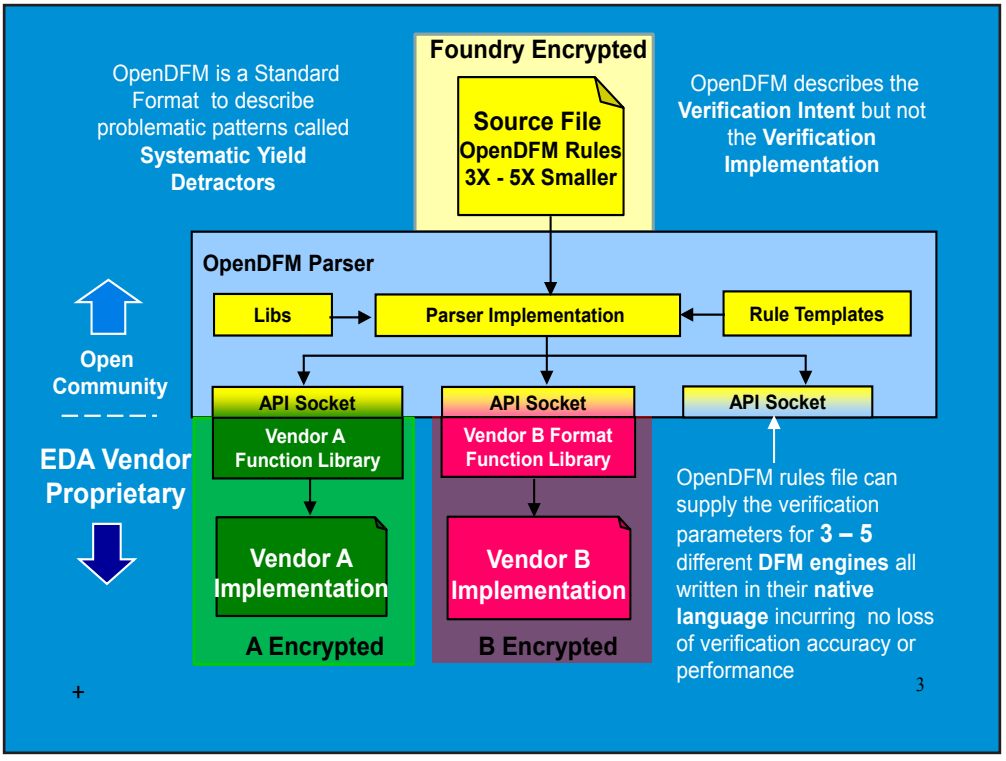
The fact that OpenDFM rules are really Tcl procedures and that the Tcl interpreter is the core of the OpenDFM parsing engine offers several syntax advantages:

• Extending the OpenDFM format to add a new rule only requires adding a new Tcl procedure and a new rule template. A rule's template defines the rule's default values, datatype constraints, parameter relationships and error messages to the library pro¬cedure that implements the rule. The OpenDFM parser itself does not have to change when a new rule was added.

• Adding a new plug-in to translates OpenDFM rules into the native format of the target verification tool, requires the development of a Tcl package that implements a plug-in translator. The OpenDFM parser itself does not require any modification to extend the translation of OpenDFM rules into a new verification format.

• The OpenDFM parser provides a standard API for all translator plug-ins. The OpenDFM plug-in interface meets the legal requirements that any plug-in translator can easily be substituted for another and that all plug-ins have access to the same informa¬tion from the OpenDFM parser.

• As shown below, OpenDFM rules files are typically 3X – 5X smaller than the native rules files of commercial physical verification engines. This is because OpenDFM rules only describe the verification intent and not the steps to perform the physical verification. A single OpenDFM rule files can provide the verification intent for 3 – 5 different physical verification engines. With these two advantages, OpenDFM can reduce the unit volume of the DRC rules (the total lines of DRC rules for a project) required for physical verification by 10X – 20X.



Standards Viewpoint

The Role Of Adoption Aids In The Standards World

Steve Schulz
President & CEO, Si2

When I came over to Si2 after 20+ years in the semiconductor industry, I was critical of how many standard specifications were created and approved, but then poorly adopted. My main point was, and remains, that there is no commercial value to a standard until widely adopted, so the industry needed process improvement applied to how we go about ensuring our investments are not wasted. Part of that process is clarity and alignment of need for a proposed standard – who needs it, and when it must be ready. Too early and it has no market; too late, and the concrete of "incompatibility chaos" has set and dried. Another aspect is supporting the life cycle needs of a standard through adoption – what is required to remove barriers that prevent rapid and consistent adoption across industry?

Creation of a specification is one thing, but adoption is another, often more difficult, challenge. Adoption aids for a standard may include education, training, test cases, labs, parsers, header files, or even a full "reference implementation" or "reference flow". Sometimes, supporting software may provide useful bindings to popular scripting languages, enable translation among other formats and APIs, and might include value-added utilities to aid integration testing, debugging, and data inspection / analysis. Website support for adoption should consider offering on-line discussion forums, bug trackers, and new feature requests. In addition, new contributions of technical requirements, data models, or code implementations may require appropriate licenses, "certificates of authenticity", and legal protections for all other participating members. Finally, effective standards development needs to work acceptably well in a global context – which may mean multiple languages and widely-varying time zones.

Not all standards require such heavy lifting. For example, Si2's ECSM Noise standard is a mere 31 pages, describing straightforward file format syntax. By contrast, OpenAccess includes nearly 700 C++ classes, dozens of information model diagrams, plus over 1100 pages that define the API standard. This standard is supported by over 1.5 million lines of code, updated multiple times each year (along with training, labs, etc). OpenAccess could not have succeeded without this strong and consistent support.

Most standards will fall somewhere in between those extremes. The key point: plan for adoption as part of the development of the standard to avoid wasting resources. This does not mean that success of a standard is assured – many external variables come into play, just as with any product introduced into a market. One of the ways to improve the odds is through a large and broad set of active stakeholders working together on the open standard, with equal rights and equal opportunities.

Industry Events

ICCAD 2011 (Si2 - Corporate Sponsor)

Nov. 7-10, San Jose, CA: The International Conference on Computer-Aided Design (ICCAD) is the world's premier conference devoted to technical innovations in design automation of devices, circuits, and systems and has served EDA and Design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. ICCAD remains uniquely recognized as the place where the most in-depth and respected research work in EDA is presented. For more information, go to http://iccad.com/home

9th International SOC Conference (Si2 - Co-Sponsor)

Nov. 2 &3, Newport Beach, CA: The 9th International SoC Conference, Exhibit & Workshops will be held at the Radisson Hotel Newport Beach (California) and will offer two days of technical presentations, panel discussions, tabletop exhibits, tutorials, and a variety of technical workshops. Over the past 8 years, the International SoC Conference has established itself as the premier annual event for System-on-Chip and VLSI. The Conference provides an outstanding platform for sharing and disseminating groundbreaking research, revolutionary product announcements, and innovative technical tutorials, and it has established itself as the forum for debating emerging challenges in System-on-Chip, VLSI, and Nanotechnologies.
For more information on the conference: http://socconference.com/index.htm

Much of the information in this newsletter is the direct result of the extensive effort put forth by Si2 member companies in the many Working Groups in the various Coalitions. We extend our sincere appreciation for their contributions.

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