

## Where the Real Work gets done *Coalition Working Groups lead the way*

Where do Standards really come from? Who does all the research, analysis and negotiation to develop a workable solution to an industry problem?

At Si2, the answer is Working Groups. Each of the four major projects, the OpenAccess Coalition, the Low Power Coalition, the Design for Manufacturability Coalition and the Open Modeling Coalition have their own subset of Working Groups (WG) which define alternatives to resolve the problems identified by the Coalition itself. Coalition members volunteer resources such as manpower and/or technical donations to help resolve the issue. The diagram on the left shows how the Coalitions and WGs are organized. In this newsletter we'll look at some the specific projects going on in the WGs.

### Report from the Si2/GSA 3D Standards Workshop

The Si2-GSA 3D Standards Workshop was held at the Santa Clara Convention Center on 10/1/2009. There were almost 50 attendees representing all stakeholders from the semiconductor industry, as well as members from academia and other standards organizations. The workshop attendees heard presentations from all the stakeholders and collected a treasure trove of information and requirements for standards that are being compiled and assimilated at the present time. The important message drawn from this workshop is that modeling of through-silicon-vias (TSV's) is a significant challenge and that 3D design will not only require significant enhancements to existing design flows and tools for 2D design but will require new methods for design exploration and implementation across a third dimension as well as methods to access analysis tools for mechanical and thermal stress. The formal presentations will be available from websites of Si2 and GSA while the requirements gathered at the workshop will form the basis for future work on standards development activities at Si2 and other partner organizations.

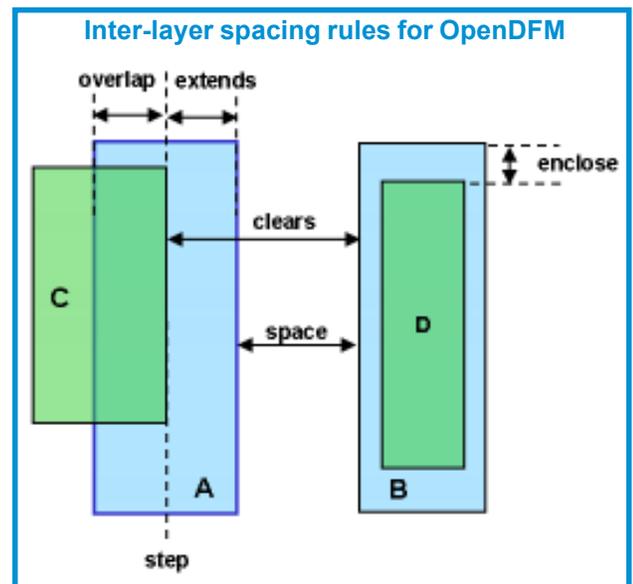
### Coalition Working Groups develop specific aspects of a Standard

#### OpenDFM Specification Working Group

The OpenDFM specification working group is reviewing a near final draft of a universal DRC language that can be translated into a variety of proprietary verification languages such as those for tools like Calibre, Hercules and Quartz, with no loss of accuracy or performance. Recent DAC demos indicate that the OpenDFM format has the potential to reduce the volume of DRC rules by 10X – 20X because it describes physical verification at a higher level than traditional DRC rules. The DFMC is focused on the completion of OpenDFM which is scheduled for release later this year with rapid adoption expected by all major EDA vendors, silicon foundries, and end-user companies. The next release of openDFM will add rules for Lithography, Chemical Mechanical Planarization and Critical Area Analysis.

One instance of the complexity of DFM rules lies in spacing rules for the newest technology nodes. Spacing rules at 32nm process nodes depend on many factors including the length and width of the neighboring shapes as well as interactions with other layers such as an overlap of metal 2 with metal 1.

OpenDFM provides a compact notation for the description of physical verification rules that include conditional rules and ranges of acceptable values.

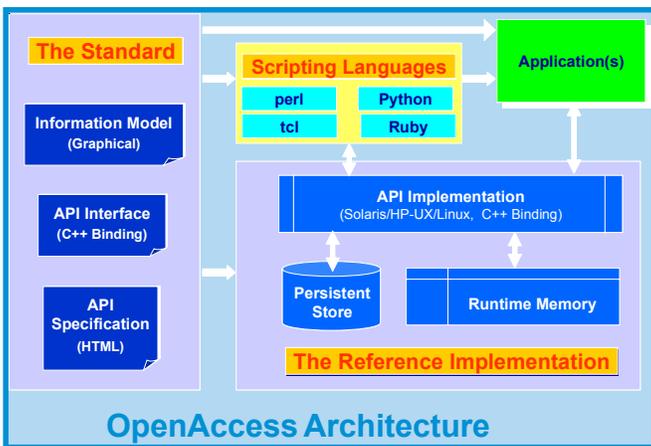


# OpenAccess Coalition

## Scripting Languages Working Group

The Open Access Coalition has started a Scripting Languages Working Group (WG). The charter of the WG is to define a process for creating OA interfaces to popular scripting languages which include: Python, Perl, TCL, and Ruby. This WG will endeavor to define a common architecture for the different language translators, and simplify and standardize the building and maintenance of scripted interfaces as much as possible. Most OpenAccess API methods should automatically be supported without hand coding through templates, code generators, etc.

The group will also provide suggestions to the OpenAccess ChangeTeam about API changes that would make the different scripting language interfaces easier. Guidelines for each language will include means by which it may be true to the OA interface (docs for OA C++ interface



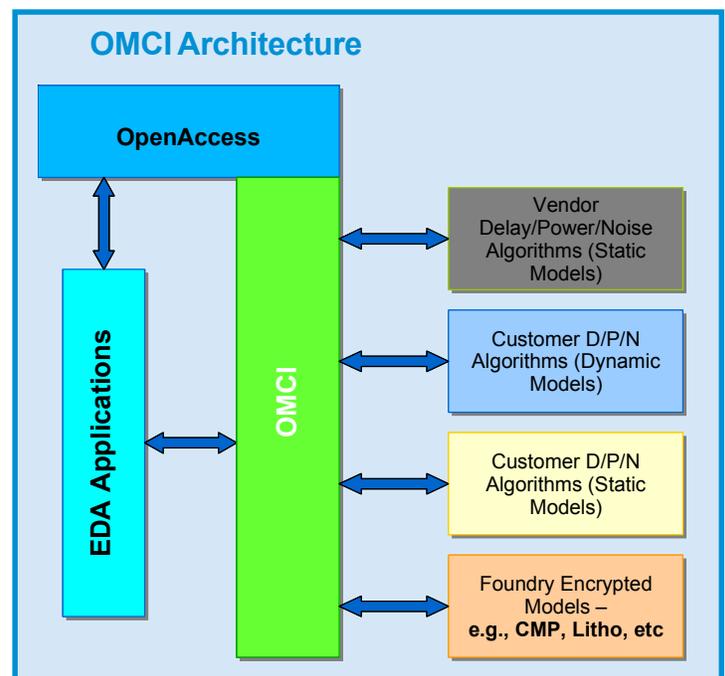
should match each language API closely) and being true to the native language look-and-feel (iterators, exceptions, etc. done in a native way). The expectation is that the WG will collaborate on overall techniques and divide the effort for individual languages. The exact list of supported languages depends on WG members' preferences and interests. The working group is still recruiting interested companies and individuals. If you have an interest, please contact [nenglish@si2.org](mailto:nenglish@si2.org) for more information.

## Joint Data Model Working Group

This WG, which has been in operation for about 2 years, is an example of the synergies that exist between the OpenAccess Coalition and the Open Modeling Coalition.

The International Technology Roadmap for Semiconductors (ITRS) 2007 Modeling and Simulation chapter best summarizes a modeling challenge: "To support heterogeneous integration, CAD-tools must be enhanced to better handle simulations with different technologies and in different simulation and application domains (RF, digital and mixed signal). They will need to handle multiple interactions between circuit models, building block models, interconnect, dies and packages... To allow for the increasing complexity and interactions of the IC-package-PCB system, a modular approach that allows for different implementations of different component models may likely be required, especially when considering system-in-package or system-on-chip solutions. It may be necessary to simultaneously consider digital, analog, RF, and even micro-electro-mechanical systems (MEMS) and optical components..."

The quote above serves as an important statement of need for an architecture similar or identical to the Open Modeling Calculation Interface (OMCI) shown in the accompanying illustration. OMCI is a modular programming interface that allows the separation of any given model (provider) from its application (consumer) and which provides syntactic and semantic clarity and consistency.



OMCI is designed initially to provide a single universal modeling interface for timing, power and noise analysis by leveraging existing Si2 standards such as OpenAccess and ECSM and to serve as a basis for other OpenAccess modeling interfaces, such as, for importing DFM models or behavioral models at the Electronic System Level (ESL). This modular approach is expected to improve consistency of results between different applications in a design flow, including timing, noise, and power analysis. This will also eliminate calculation (algorithm) disparities as a design is moved through the flow since consistent model interpretation by applications from different vendors is now possible since the same delay, power, and noise calculators can be shared by all applications. In addition, the library owner can now control correlation between low accuracy (fast runtime) and high accuracy (slower runtime) modes available in the same delay calculator. The Joint Data Model Working Group manages the evolution of the OMCI within the Open Modeling Coalition of Si2.

# Open Modeling Coalition

## Characterization and Validation Working Group

The Characterization and Validation WG of the Open Modeling Coalition recently published a new Si2 Standard for Characterization Extensions to the Liberty Specification. This Standard defines a common Liberty syntax for exchanging simulation settings and measurement choices that affect characterization data. The standard will enable library providers to state how they configured the environments and measurements for library characterization. And, it will enable library users to avoid misalignments between design settings and the characterization environment. By enabling the sharing of characterization setup information, the standard will assist library validators to solve deviations between static analysis and SPICE results caused by incorrect validation and correlation setups. This is an important step forward because currently, characterization settings are not included in libraries. This information is needed for re-characterization, for re-targeting, and for down-flow tool setups. All attributes in the proposed extensions are optional so Liberty files will remain valid even when these settings are not defined. This is an important new contribution to the industry and is one that will ease the use of libraries throughout the design flow. Those interested in more information may download the released specification at <https://www.si2.org/openeda.si2.org/projects/omcdistrib/>



**Liberty Extension Proposals**

**Fourteen Categories**

<b>Environment References</b>	<b>Dynamic Power Measurements</b>
<b>Simulator Settings</b>	<b>Input Pin Power Measurements</b>
<b>Input waveform</b>	<b>Leakage Power Measurements</b>
<b>Process Models</b>	<b>Constraints Settings</b>
<b>Load Selection</b>	<b>Capacitance Settings</b>
<b>Timing Measurements</b>	<b>Tristate Delay &amp; Slew Settings</b>
<b>Current Source Models</b>	<b>External Harness Circuits</b>

**Seventy Six Specific Proposals in these Categories**

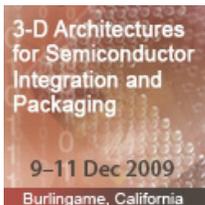
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## Industry Events



### 3-D Architectures Conference (Si2 Co-Sponsors)

Industry leaders will speak at RTI International's fourth international conference "3-D Architectures for Semiconductor Integration and Packaging" in San Francisco Dec. 9-11. Held annually since 2002, this conference series has become recognized as the premier gathering of senior technologists and business leaders involved in 3-D integration and packaging. This year's event features nearly 30 invited speakers during the conference and pre-conference symposium, presenting on the impact of the latest technology and market developments.

This year's conference will provide attendees and speakers the unique opportunity to explore and understand the technology and business implications of the trend toward 3-D device and system integration in the semiconductor industry. Conference Sessions for this year's event include: The IDM and Foundry Perspective on 3-D Technology Trends and Opportunities, The Packaging Foundry and its Vital Role in Driving 3-D, Looking Over the Horizon - Forecasting Growth, On the Front - Applications Driving 3-D Development and Commercialization, Taking Advantage of 3-D - Rethinking Design Approaches, Industry and Government Funded 3-D Efforts - Key Research Outcomes and Resources, Fundamental Technology Approaches to Building 3-D, Wafer Handling Leads the Way on Manufacturing. Visit their website for more details: <http://techventure.rti.org>.



### ICCAD 2009 (Si2 - Corporate Sponsors)

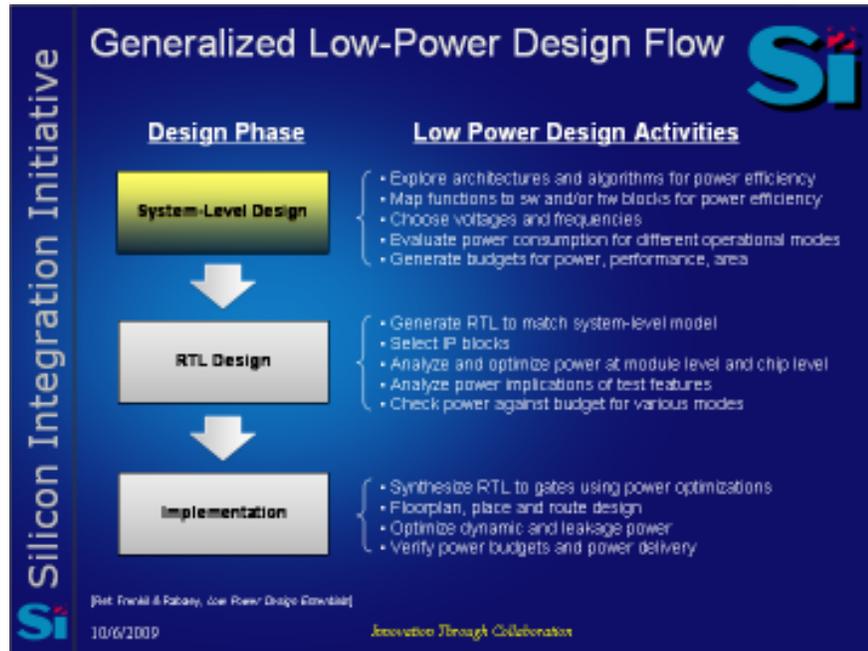
The International Conference on Computer-Aided Design (ICCAD) is the world's premier conference devoted to technical innovations in design automation of devices, circuits, and systems and has served EDA and Design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. ICCAD remains uniquely recognized as the place where the most in-depth and respected research work in EDA is presented. For more information, go to <http://www.iccad.com/2009/index.html>

# Low Power Coalition



## Modeling Working Group

The lack of structured high-level modeling capabilities hinders power analyses during early design phases. The Modeling Working Group of the Si2 Low Power Coalition has begun to codify requirements and have prepared an outline for a multi-layer power modeling proposal. The proposed structure should be applicable to a wide range of functional complexity as well as a variety of simulation styles. Future work has been identified with the goal of preparing a formal Modeling Requirements document. This topic is very timely, since more formalism at the ESL level is developing, especially with respect to TLM modeling. The goals are to enable power tradeoffs during system level design & simulation, and to enable the earliest possible view of system power characteristics. Some power models exist for IP blocks, but they are difficult to generate (characterize and model). Current modeling constructs are inadequate for representing complex power behavior and they are often incomplete, inaccurate, or both. To compound the problem, models are often non-transportable between applications. Now, power modeling capabilities exist for low level primitives (Liberty), but they are not sufficient for high level modeling. The Working Group is looking at recommending format extensions to aid in power modeling. This is not intended to replace Liberty models, but to extend or complement them. These format recommendations may also apply to other existing formats (e.g. CPF, UPF, Liberty, TLM, IPEXact)



**Interoperable Subset Analysis: An Example**

IEEE 1801-2009	CPF 1.1
<b>set_retention</b>	<b>create_state_retention_rule</b>
retention_name	-name string
-domain domain_name	-domain power_domain
[-elements element_list]	-instances instance_list
[-exclude_elements exclude_list]	-exclude_instance_list
[-retention_supply_set ref_supply_set]	[-secondary_domain domain]
-save_signal {{{logic_net <high low posedge negedge>}}	-save_edge expr
	-save_level expr
-restore_signal {{{logic_net <high low posedge negedge>}}	-restore_edge expr
	-restore_level expr
[-save_condition {{{boolean_function}}}]	[-save_precondition expr]
[-restore_condition {{{boolean_function}}}]	-restore_precondition expr]
<b>[-retention_condition {{{boolean_function}}}]</b>	
	<b>[-target_type {nopatch both}]</b>

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## Format Working Group

The Format Working Group of the Si2 Low Power Coalition has published two Si2 standards: CPF 1.0 and 1.1. The group is currently continuing their work on CPF 1.2 with an emphasis on interoperability with IEEE 1801-2009. During their weekly meetings, they continue their interoperability analysis between CPF 1.1 and IEEE 1801-2009. For the rest of the year, they will focus on an Interoperability Guidelines document to be published to the industry and CPF 1.2 requirements that will lead to the CPF 1.2 Standard release. Details of the work include identifying an interoperable subset of commands and options between CPF 1.1 and IEEE 1801-2009 to be able to consistently describe a design to drive verification and implementation and to be easily supported by tools from multiple vendors. In line with this, the group has already released a document to the P1801 WG to establish a common understanding of location of isolation cells. It will soon publish the interoperability guidelines as

a starting point for companies to adhere to so that designers can develop best-in-class low power design flows to meet their specific design challenges. The document will also provide guidance for commands outside of the interoperable subset as well as recommendations for future CPF and IEEE 1801-2009 extensions.

Corporate site: [www.si2.org](http://www.si2.org)  
Downloads: [www.openeda.si2.org](http://www.openeda.si2.org)

