3D Interconnect Architectures Glossary

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3D INTERCONNECT ARCHITECTURES

INTRODUCTION

New developments in electronic system integration look increasingly to the third dimension for a variety of reasons, such as miniaturization, heterogeneous integration, improved circuit performance and lower power consumption. A broad variety of technologies is proposed by all players in the electronic manufacturing supply chain (IC foundry → wafer level processing (WLP) → semiconductor assembly and test (SAT) → printed circuit board (PCB) → assembly…), often blurring the traditional interfaces between them.

In order to come to a clear vision on roadmaps for 3D technologies, it is important to come to a clear definition of what is understood by 3D interconnect technology and to propose a classification of the wide variety of technologies. This definition should capture the functional requirements of 3D technology at the different hierarchical levels of the system and correspond to the supply chain manufacturing capabilities.

3D-INTERCONNECT TECHNOLOGY DEFINITIONS

When breaking down any electronic system into its basic components—the transistors, diodes, passive circuit elements, MEMS, etc.—we observe that electronic systems consist of two parts: thebasic components and the highly complex interconnect fabric linking them. This interconnect fabric is organized in a hierarchical way, from narrow short interconnects between basic elements to longer and larger interconnects for interconnecting circuit blocks. For integrated circuits with well-defined local, intermediate and global interconnect layers, on chip circuit-hierarchy is organized from transistors to logic gates, sub-circuits, circuit-blocks, and finally, bond pad interface circuits. This is also the case for electronic systems as a whole, which typically consist of multiple integrated circuits, passive components, crystals, MEMS, etc., and which also are organized in different levels corresponding to, for example, the IC-package, system-on-package, module, board, rack, level. An example is the classification according to JISSO.[1]

Within a certain level of the interconnect hierarchy, interconnects are essentially routed in a 2D-topology: isolated lines are defined on a surface without crossing each other. Crossing of lines are realized on adjacent interconnect planes. Connections between planes are realized through features, such as vias, plated through holes, pins, solder balls, and/or connectors. These "via" interconnects allow for the 3D stacking of interconnect levels. The combination of basic circuit elements with multiple 2D-interconnect planes is considered a 2D-device, such as the integrated circuit or the printed circuit board.

What is commonly considered a "3D technology" today is a different type of "via" technology that allows for the stacking of basic electronic components in the third dimension, not only interconnect planes. This is the main distinctive feature of 3D integration technologies. It allows for the realization of electronic systems with very high packaging efficiency, measured either per unit area or per unit volume.

3D DEFINITIONS AND NAMING CONVENTIONS

3D Interconnect Technology—technology which allows for the vertical stacking of layers of basic electronic components that are connected using a 2D-interconnect fabric are as follows:

- "Basic electronic components" are elementary circuit devices such as transistors, diodes, resistors, capacitors and inductors.
- A special case of 3D interconnect technology is the Si interposer structures that may only contain interconnect layers, although in many cases other basic electronic components (in particular decoupling capacitors) may be embedded.

3D Bonding—operation that joins two die or wafer surfaces together

[1] *http://jisso.ipc.org*

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3D Stacking—operation that also realizes electrical interconnects between the two device levels

3D-Packaging (3D-P)—3D integration using "traditional" packaging technologies, such as wirebonding, package-on-package stacking or embedding in printed circuit boards.

3D-Wafer-Level-Packaging (3D-WLP)—3D integration using wafer level packaging technologies, performed after wafer fabrication, such as flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging, and fan-out reconstructed wafer chip-scale packaging

3D-System-on-chip (3D-SOC)—Circuit designed as a system-on-chip, SOC, but realized using multiple stacked die. 3D-interconnects directly connect circuit tiles in different die levels. These interconnects are at the level of global on-chip interconnects. This allows for extensive use/reuse of IP-blocks.

3D-Stacked-Integrated-Circuit (3D-SIC)—3D approach using direct interconnects between circuit blocks in different layers of the 3D die stack. Interconnects are on the global or intermediate on-chip interconnect levels. The 3D stack is characterized by a sequence of alternating front-end (devices) and back-end (interconnect) layers.

3D-Integrated-Circuit (3D-IC)—3D approach using direct stacking of active devices. Interconnects are on the local on-chip interconnect levels. The 3D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack.

Table INTC1 presents a structured definition of 3D interconnect technologies based on the interconnect hierarchy. This structure also refers to the industrial semiconductor supply chain and allows definition of meaningful roadmaps and targets for each layer of the interconnect hierarchy. [1]

Table INTC1 3D Interconnect Technologies Based on the Interconnect Hierarchy

Level	*Suggested Name*	*Supply Chain*	*Key Characteristics*
Package	3D-Packaging (3D-P)	OSAT Assembly PCB	▪ Traditional packaging of interconnect technologies, e.g., wire-bonded die stacks, package-on-package stacks. ▪ Also includes die in PCB integration ▪ No through-Si-vias (TSVs)
Bond-pad	3D-Wafer-level Package (3D-WLP)	Wafer-level Packaging	▪ WLP infrastructure, such as redistribution layer (RDL) and bumping. ▪ 3D interconnects are processed after the IC fabrication, "post IC-passivation" (via last process). Connections on bond-pad level. ▪ TSV density requirements follow bond-pad density roadmaps.
Global	3D-Stacked Integrated Circuit/ 3D-System-on-Chip (3D-SIC /3D-SOC)	Wafer Fab	▪ Stacking of large circuit blocks (tiles, IP-blocks, memory –banks), similar to an SOC approach but having circuits physically on different layers. ▪ Unbuffered I/O drivers (Low C, little or no ESD protection on TSVs). ▪ TSV density requirement significantly higher than 3D-WLP : Pitch requirement down to 4-16µm
Intermediate	3D-SIC	Wafer Fab	▪ Stacking of smaller circuit blocks, parts of IP-blocks stacked in vertical dimensions. ▪ Mainly wafer-to-wafer stacking. ▪ TSV density requirements very high: Pitch requirement down to 1-4 µm
Local	3D-Integrated Circuit (3D-IC)	Wafer Fab	▪ Stacking of transistor layers. ▪ Common BEOL interconnect stack on multiple layers of FEOL. ▪ Requires 3D connections at the density level of local interconnects.

3D-THROUGH-SI-VIA TECHNOLOGY DEFINITIONS

A wide variety of technologies can be used to realize the 3D interconnect technologies described above. Of particular interest here are the so-called "Through-Si-Via" technologies used for 3D-WLP, 3D-SOC, and 3D-SIC interconnect technologies.

A Through Silicon Via connection is a galvanic connection between the two sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections. The isolation layer surrounding the TSV conductor is called the *TSV liner*. The function of this layer is to electrically isolate the TSVs from the substrate and from each other. This layer also determines the TSV parasitic capacitance. In order to avoid diffusion of metal from the TSV into the Si-substrate, a *barrier layer* is used between the liner and the TSV metal.

Numerous methods have been proposed for realizing these TSV-stacked 3D-SIC and 3D-WLP structures. Common to all these approaches are three basic technology modules:

1. The Through-Si-Via process
2. Wafer thinning, thin wafer handling, and backside processing
3. The actual 3D-stacking process

The sequence of these process modules may vary, resulting in a large variation of proposed process flows, as shown in Figure INTC1.

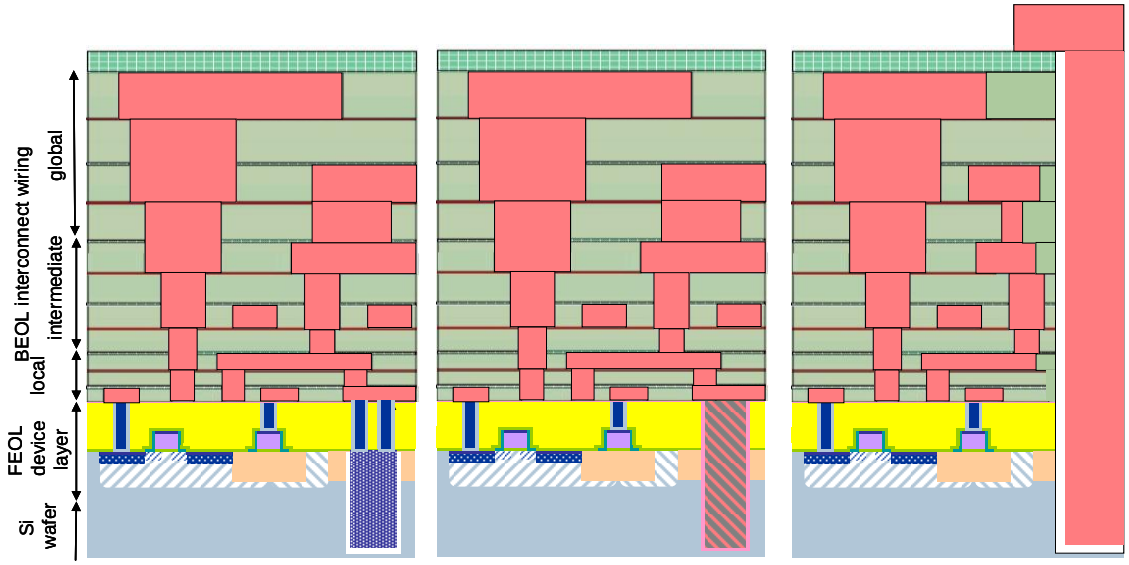

Figure INTC1 Schematic Representation of TSV First, Middle and Last Process Flows

The different process flows may be characterized by four key differentiating characteristics:

1. The order of the TSV process with respect to the device wafer fabrication process: (see Figure INTC1)
   - *"Via-first"*—fabrication of TSVs before the Si front-end of line (FEOL) device fabrication processing.

- *"Via-middle"*—fabrication of TSVs after the Si FEOL device fabrication processing but before the back-end of line (BEOL) interconnect process,
- *"Via-last"*—fabrication of TSVs after or in the middle of the Si BEOL interconnect process.

2. The order of TSV processing and 3D-bonding—TSV before or after 3D-bonding[2]
3. The order of wafer thinning and 3D-bonding—Wafer thinning before or after 3D-bonding.
4. The method of 3D-bonding:
   - Wafer-to-wafer (W2W) bonding
   - Die-to-wafer (D2W) bonding
   - Die-to-die (D2D) bonding

In addition to these four main characteristics, three secondary characteristics are identified:

- *Face-to-Face* (F2F) or *Back-to-Face* (B2F) bonding
- For "via-last": "*Frontside*" TSVs realized starting from the top surface of the wafer or "*Backside*" TSVs starting from the thinned wafer backside. (The top surface of the wafer being the side with the active devices and back-end interconnect layers)
- Removal of the carrier-wafer before or after bonding (i.e., temporary bonding and permanent bonding).

The generic flow characteristics defined above are applicable to 3D-WLP and global and intermediate interconnect level 3D-SIC process flows. For 3D-WLP TSV technology, the via-last route is the most important and is realized before 3D bonding either as frontside or backside TSV, as shown in Figure INTC2.

The different approaches presented are not only applicable to regular semiconductor devices, but can also be applied to passive redistribution or interposer substrate layers. Key processing technologies for 3D integration are the various temporary or permanent bonding and debonding operations. The requirements for the materials and processes used may vary significantly, depending on the chosen route.

[2] *In literature, sometimes TSV processing after 3D bonding is also referred to as "via last" technology. We however define "via last" in relation to the semiconductor wafer fabrication process, which makes the "via last" definition more general and not restricted to TSV after 3D bonding only.*

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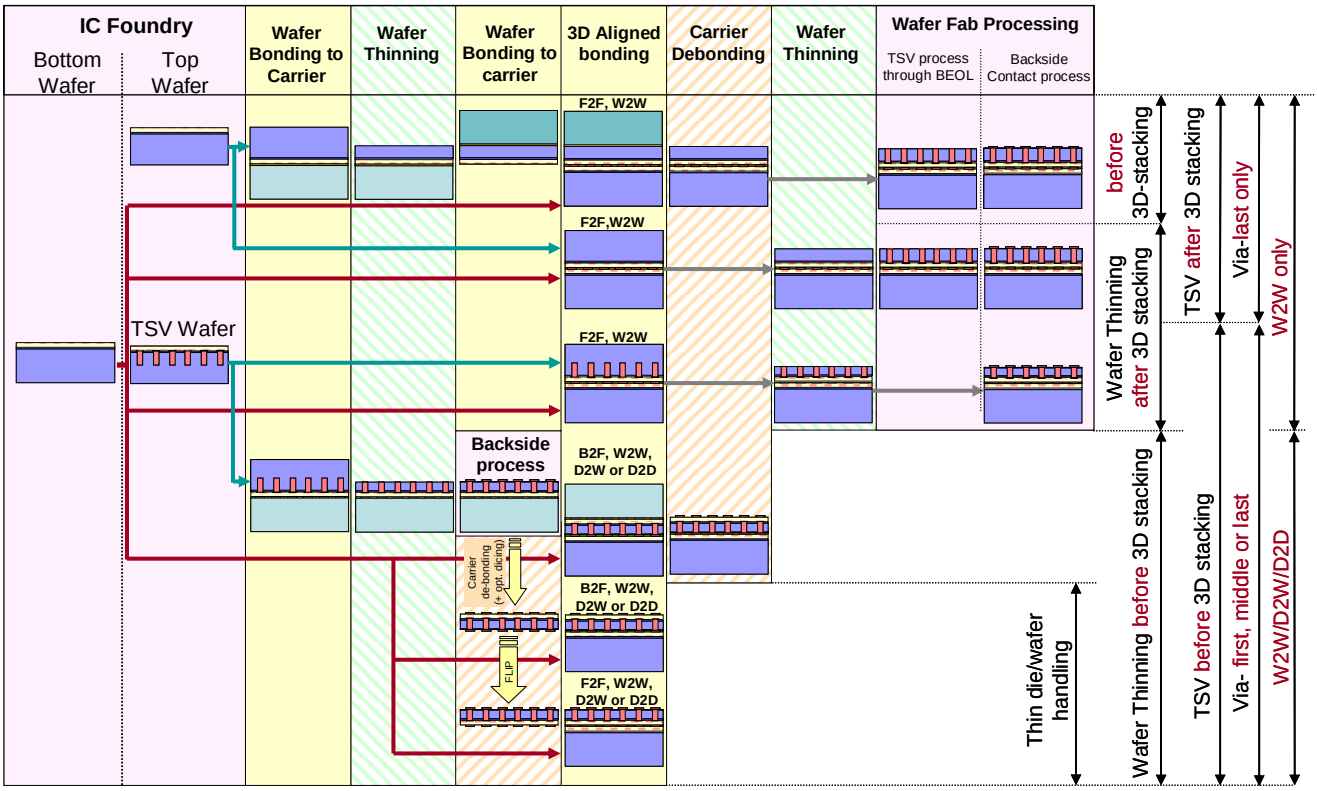

Figure INTC2 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-SIC Technologies[3]

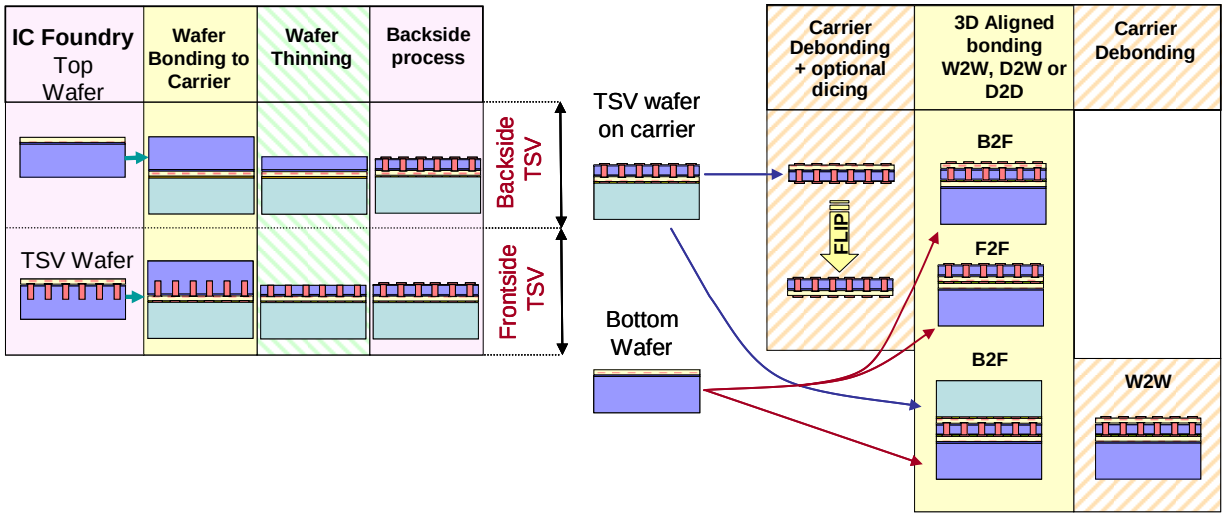

Figure INTC3 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-WLP Technologies[4]

[3] *IMEC*
[4] *IMEC*

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GLOSSARY OF 3D AND TSV DEFINITIONS

3D interconnect technology—Technology which allows for the vertical stacking of layers of basic electronic components that are connected using a layer 2D-interconnect fabric.

3D Bonding—An operation that joins two or more die or wafer surfaces together.

3D Stacking—3D bonding operation that also realizes electrical interconnects between the device levels.

3D-System-In-Package (3D-SIP)—3D integration using "traditional" packaging technologies, such as wire bonding, Package-on-package stacking or embedding in printed circuit boards.

3D-Wafer-Level-Packaging (3D-WLP)—3D integration using wafer level packaging technologies, performed after wafer fabrication, such as flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging and fan-out reconstructed wafer chip-scale packaging.

3D-System-on-chip (3D-SOC)—Circuit designed as a system-on-chip, SOC, but realized using multiple stacked die. 3D-interconnects directly connect circuit tiles in different die levels. These interconnects are at the level of global on-chip interconnects. Allows for extensive use/reuse of IP-blocks.

3D-Stacked-Integrated-Circuit (3D-SIC)—3D approach using direct interconnects between circuit blocks in different layers of the 3D die stack. Interconnects are on the global or intermediate on-chip interconnect levels. The 3D stack is characterized by a sequence of alternating front-end (devices) and back-end (interconnect) layers.

3D-Integrated-Circuit (3D-IC)—3D approach using direct stacking of active devices. The 3D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack

Through-Si-Via connection (TSV)—A galvanic connection between both sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections.

TSV liner—The isolation layer surrounding the TSV conductor

TSV barrier layer—Barrier layer in TSV in order to avoid diffusion of metal from the TSV into the Si-substrate.

"Via-first" TSV process—Fabrication of TSVs before the Si front-end (FEOL, Front-End-Of-Line) device fabrication processing

"Via-middle" TSV process—Fabrication of TSVs after the Si front-end (FEOL) device fabrication processing but before the back-end (BEOL, Back-End-Of-Line) interconnect process

"Via-last" TSV process—Fabrication of TSVs after (or in the middle of) the Si back-end (BEOL) interconnect process.

Wafer-to-Wafer (W2W, WtW) bonding—3D-stacking strategy that uses a wafer on wafer alignment and bonding strategy. Stacked die must be equal in size and wafer stepping pattern.

Die-to-Wafer (D2W, DtW) bonding—3D-stacking strategy that uses a die on wafer alignment and bonding strategy. Stacked die can have different sizes and partial population of a wafer is possible.

Die-to-Die (D2D, DtD) bonding—3D-stacking strategy that uses a die on die alignment and bonding strategy. Stacked die can have different sizes.

Face-to-Face (F2F, FtF) bonding—3D-stacking strategy where the sides of the die or wafers with active devices (="Face"-side) face each other after bonding.

"Frontside" TSVs—TSVs realized starting from the top surface of the wafer 5device and interconnect side of the wafer) .

"Backside" TSVs—TSVs starting from the thinned wafer backside.

Back-to-Face (B2F, BtF) bonding—3D-stacking strategy where the backsides of the die or wafers face each other after bonding.

Outer TSV-Aspect ratio—Ratio depth of the TSV to the maximum diameter of etch hole in the Si substrate.

Inner TSV-Aspect ratio—Ratio depth of the TSV to the maximum diameter of conductive layer of the TSV. (Aspect ratio, excluding the liner thickness)

ADDITIONAL DEFINITIONS FOR 2.5D & 3D TECHNOLOGY

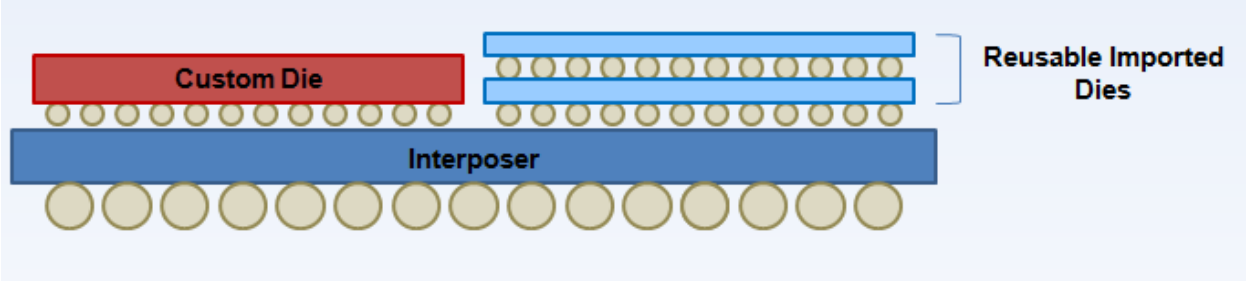
(CONTRIBUTED BY SI2 OPEN3D TECHNICAL ADVISORY BOARD)

Interposer – A substrate used for interconnecting multiple die, die stacks and passive components. Substrates can be made of silicon, glass or other materials. Silicon interposers by nature can be either passive or active.

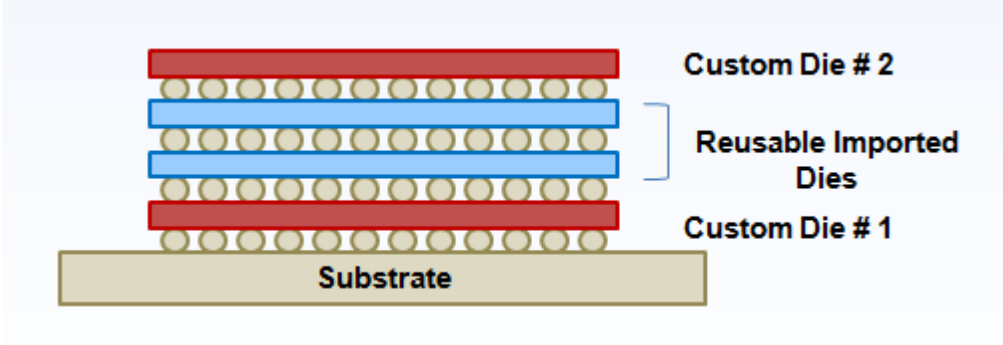
Re-Usable Die— Typically designed for use in multiple applications, such as a 3D stack or a 2.5D interposer-based package. Typically designed by a separate entity, often before a stack where it will be used is designed. (e.g., Wide IO DRAM)

Custom Die—Typically designed for use in a specific 3D stack or 2.5D interposer-based package (e.g., a digital SoC die)

3D Stack – Integration typically of multiple dies including one or more custom dies. Usually designed together with the custom die(s) for a given integration scheme and application (e.g., the schemes illustrated below)



2.5D Stack: Integration of multiple die (and/or homogenous die stacks) side-by-side on silicon or glass interposer



***3D Stack*:** Integrating multiple heterogeneous die on top of each other in a conventional package